ARMY TM 11-5895-389-34-1
NAVY NAVELEX 0967-LP-377-7020
AIR FORCE TO 31R5-2TSC54-22-1

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL

SATELLITE COMMUNICATION TERMINAL AN/TSC-54 (FUNCTIONAL ANALYSIS) (NSN 5895-00-937-4993)

This copy is a reprint which includes current pages from Changes 1 through 3.

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

JANUARY 1978

The following are general safety precautions that are not related to any specific procedures and, therefore, do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

WARNINGS

Maintenance personnel should be familiar with the safety requirements before attempting maintenance or operation of the equipment covered by this manual. Failure to follow requirements and observe safety precautions could result in injury or DEATH.

HIGH VOLTAGE is used in this equipment. DEATH ON CONTACT may result if safety precautions are not observed. Don't take chances.

DANGEROUS VOLTAGES EXIST IN THE FOLLOWING UNITS:

Electronic Equipment Shelter S-378/TSC-54	208 volts ac
Trailer-Mounted Diesel Engine Generator Set	208 volts ac
Antenna-Receiver-Transmitter Group OA-8244/TSC-54	208 volts ac
	-13,000 volts dc

The shelter must be ventilated at all times when occupied by personnel. Open the exhaust vent and air intake doors and operate the blower fans for ventilation.

Under no circumstances should any personnel reach within or enter an equipment inclosure for the purpose of servicing or adjusting the equipment without the immediate presence or assistance of another person capable of rendering aid.

Exhaust gases produced by diesel engine generator sets are POISONOUS. Inhalation may result in illness or DEATH. Provide adequate ventilation if the generator sets are operated in inclosed or covered areas. Exhaust gas pickup by air conditioners should be carefully avoided.

Do not operate or perform maintenance on the generator sets without a suitable ground connection. Electrical defects in the unit, load lines, or load equipment can cause DEATH by electrocution when contact is made with an ungrounded system.

Maintenance personnel should be familiar with the requirements of TB SIG 291 before attempting maintenance on the antenna.

In troubleshooting, it may be necessary to close interlock switches with a unit inclosure open. Extreme care must be observed under such conditions to avoid physical contact with live circuits. This equipment employs voltages which are dangerous and may prove FATAL if proper safety precautions are not observed.

Performance of any field expedient repair creates a condition possibly dangerous to equipment and personnel. The equipment so repaired, should be taken out of service as soon as possible for replacement of the defective parts.

The C-field and 1 PPS of the cesium beam frequency standard will not be adjusted except by direction from the U.S. Naval Observatory (NAVOBSY). The NAVOBSY will give the new setting of the C-field dial control or the six TIME DELAY thumbwheel switches to be adjusted. The instructions and procedures for the operation and reporting of data is contained in the NAVOBSY TS/TT1-O/M.

TM 11-5895-389-34-1
NAVELEX 0967-LP-377-7083
TO 31R5-2TSC54-22-1
C3

Change
No. 3

DEPARTMENTS OF THE ARMY,
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Washington, DC, 2 *February 1981*

Direct Support and General Support Maintenance Manual

SATELLITE COMMUNICATION TERMINAL AN/TSC-54

(FUNCTIONAL ANALYSIS)

(NSN 5895-00-937-4993)

TM 11-5895-389-34-1 NAVELEX 0967-LP-377-7020/TO 31R5-2TSC54-22-1, 5 January 1978, is changed as follows:

1. Changed material on illustrations is indicated by a pointing hand.

2. Remove old pages and insert new pages as indicated below:

Remove	*Insert*
Figure FO 2-3 (sheet 4)	Figure FO 2-3 (sheet 4)
Figure FO 2-10	Figure FO 2-10

3. File this change sheet in front of the manual for reference purposes.

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Change No. 2

DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE
Washington, DC, 10 June 1980

Direct Support and General Support Maintenance Manual

SATELLITE COMMUNICATION TERMINAL AN/TSC-54

(FUNCTIONAL ANALYSIS)

(NSN 58960-9374993

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Remove	*Insert*
1-3 through 1-6.	1-3 through 1-7
2-29 and 2-30	2-29 and 2-30
2-33 and 2-34	2-33 and 2-34
2-49 and 2-50	2-49 and 2-50.1
None	Figure FO 2-2 (sheet 14.1)
Figure FO 2-9 (sheet 1)	Figure FO 2-9 (sheet 1)

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Rear Admiral, United States Navy
Commander, Naval Electronic Systems Command

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CHANGE 1
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No. 1

DEPARTMENTS OF THE ARMY,
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Remove	*Insert*
i and ii	i and ii
2-11 through 2-20	2-11 through 2-20
2-23 through 2-26	2-23 through 2-26
None	Index- 1 and Index 2
None	Figure FO 2-1 (sheet 7.1)
Figure FO 2 -1 (sheet 12 of 16)	Figure FO 2-1 (sheet 12 of 16)
Figure FO 2-1 (sheet 14 of 16)	Figure FO 2-1 (sheet 14 of 16)
Figure FO 2-2 (sheet 10 of 19)	Figure FO 2 -2 (sheet 10 of 19)
Figure FO 2-3 (sheet 1 of 9)	Figure FO 2-3 (sheet 1 of 9)
Figure FO 2 -3 (sheet 9 of 9)	Figure FO 2-3 (sheet 9 of 9)
Figure FO 2-4 (sheet 1 of 7)	Figure FO 2-4 (sheet 1 of 7)
Figure FO 2-4 (sheet 2 of 7)	Figure FO 2-4 (sheet 2 of 7)
Figure FO 2-4 (sheet 3 of 7)	Figure FO 2-4 (sheet 3 of 7)
Figure FO 2-4 (sheet 6 of 7)	Figure FO 2-4 (sheet 6 of 7)
None	Figure FO 2-4 (sheet 7.1)
Figure FO 2-7 (sheet 1 of 9)	Figure FO 2-7 (sheet 1 of 9)
Figure FO 2-7 (sheet 4 of 9)	Figure FO 2-7 (sheet 4 of 9)
Figure FO 2-7 (sheet 5 of 9)	Figure FO 2-7 (sheet 5 of 9)
Figure FO 2-7 (sheet 9 of 9)	Figure FO 2-7 (sheet 9 of 9)
Figure FO 2-8 (sheet 6 of 10)	Figure FO 2-8 (sheet 6 of 10)
Figure FO 2-9 (sheet 2 of 3)	Figure FO 2-9 (sheet 2 of 3)
Figure FO 2-10	Figure FO 2-10

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The Adjutant General

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Commander, Naval Electronics
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TECHNICAL, MANUAL
No. 11-5895-389-34-1
NAVELEX 0967-LP-377-7020
TECHNICAL ORDER
No. 31R5-2TSC54-22-1

DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE

WASHINGTON, DC *5 January 1978*

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL SATELLITE COMMUNICATION TERMINAL AN/TSC-54 (FUNCTIONAL ANALYSIS) (NSN 5895-00-937-4993)

REPORTING OF ERRORS

You can improve this manual by recommending improvements using DA Form 2028-2 located in the back of the manual. Simply tear out the self-addressed form, fill it out as shown on the sample, fold it where shown, and drop it in the mail.

If there are no blank DA Forms 2028-2 in the back of your manual, use the standard DA Form 2028 (Recommended Changes to Publications and Blank Forms) and forward to the Commander, US Army Communications and Electronics Materiel Readiness Command, ATTN: DRSEIME-MQ, Fort Monmouth, NJ 07703.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward direct to prime ALC/MST.

For Navy, mail comments to the Commander, Naval Electronic Systems Command, Training and Publications Management Office, ELEX 04F3, P.O. Box 80337, San Diego, California 92138.

In either case, a reply will be furnished direct to you.

LIST OF ILLUSTRATIONS

***This manual supersedes TM 11-5895-389-34/1, NAVSHIPS 0967-377-7020. TO 31R5-2TSC54-22, 12 February 1971 and TM 11-5895-389-34/3, NAVSHIPS 0967-377-7020, TO 31R5-2TSC54-22, 12 February 1971.**

CHAPTER 1
INTRODUCTION

Section I. GENERAL

1-1. Scope

a. This manual contains instructions for direct support and general support maintenance of Satellite Communication Terminal AN/TSC54. It includes instructions for troubleshooting, testing, alignment, repairing the equipment, and replacing specific maintenance parts. It also lists the tools, materials, and test equipment required for direct and general support maintenance.

b. The manual consists of three volumes. TM 11-5895-389-34-1 contains a functional analysis of the equipment operation and the illustrations to support this functional analysis of the equipment operation and the illustrations to support this functional analysis. TM 11-5895-389-34-2 contains a detailed circuit analysis of the equipment and the illustrations to support the detailed circuit analysis. TM 11-5895-389-34-3 contains preventive maintenance information, troubleshooting data, removal and replacement instructions, alignment procedures, general support testing information, and the index for the complete manual.

1-2. Forms and Records

a. Reports of Maintenance and Unsatisfactory Equipment. Maintenance forms, records, and reports which are to be used by maintenance personnel at all maintenance levels are listed in and prescribed by TM 38-750 (Army). Air Force personnel will use AFM 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performance utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol. 3 and unsatisfactory material/conditions (UR submissions) IAW OPNAVINST 4790.2, Vol. 2, chapter 17.

b. Report of Packaging and Hang Deficiencies. Fill out and forward DD Form 6 (Packaging Improvement Report) as prescribed in AR 700-58/NAVSUPINST 4030.29/AFR 7113/MCO P4030.29A, and DLAR 4145.8.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPTNST 4610.33B/AFR 75-18/MCO P4610.19C, and DLAR 4500.15.

1-3. Administrative Storage

Administrative storage instructions are provided in TM 740-90-1.

1-4. Destruction of Army Electronics Materiel

Demolition and destruction of electronic equipment will be under the direction of the commander and in accordance with TM 750-244-2.

1-5. Reporting Equipment Improvement Recommendations (EIR)

EIR's will be prepared using DA Form 2407 (Maintenance Request). Instructions for preparing EIR's are provided in TM 38-750, The Army Maintenance Management System. EIR's should be mailed direct to Commander, US Army Electronics Command, ATTN: DRSELMA-, Fort Monmouth, NJ 07703. A reply will be furnished direct to you.

Section II. DESCRIPTION AND DATA

1-6. Description

A description of components for the AN/TSC-54 is provided in TM 11-5895-389-12.

1-7. Equipment Analysis

a. To simplify theoretical discussion, the AN/TSC-54 has been divided into five basic component groups or systems: the transmitting system, the receiving system, the antenna control system, the control circuits system, and the power distribution system.

b. General theory of the AN/TSC-54 is

covered in a block diagram analysis (para 1-8)and detailed theory of the major assemblies is covered in a functional diagram analysis (para 2-4 through 2-76). Selected individual circuit subassemblies and modules are analyzed schematically in TM 11-5895-389-34-2.

1-8. Block Diagram Analysis

(fig. 1-1)

The AN/TSC-54 is a transportable microwave communications link terminal incorporating all ancillary items necessary for operation through satellites to other link terminals configured to the same communication satellite system. The AN/TSC-54 is capable of simultaneous transmission of two wideband carrier signals. The AN/TSC-54 provides a communication capacity of one voice circuit, and one out-of-band 100 word-per-minute (wpm) full duplex teletypewriter orderwire circuit. Multiple access and antijamming capabilities are provided by radio Communication Subsystem AN/URC-61. User service of the AN/TSC-54 is provided by local loops or by interconnection to distribution points through microwave or transmission lines. When the AN/TSC-54 is used with Communications Subsystem AN/TCC-79,, link terminal capabilities are increased by providing a maximum of 72 multiplex channels for transmission through the AN/TSC-54.

a. All input and output signals of the AN/ TSC-54 are normalized-through patch panels to their respective circuits. The voice input signal is applied to one of three selectable filters in the normal terminal configuration. The 3995-Hz tone generator is driven by a direct current (dc) signal from a line isolation unit which provides isolation between the terminal and the external user. The 3805-Hz tone generator is driven by the AN/UGC-77 teletypewriter terminal orderwire keyboard or by an external user through a line isolation unit. The 1275-Hz tone generator is primarily for use under degraded signal conditions and is not used in normal terminal configuration.

b. The voice signal and the two frequency shift keyed (fsk) tone signals (a above) are summed to form a composite baseband signal that is applied through preemphasis networks to modulator 1A3A14. The modulator provides a 70-MHz phase modulated (pm) signal which is routed to the if patch panel. Also available at this patch panel are the 70-MHz wideband inputs from the AN/URC-61 and the AN/TCC-79 when used with the AN/TSC-54.

c. The upconversion is accomplished by one of three identical upconverters. Each upconverter converts a 70-MHz signal from the if patch panel into an rf signal in the frequency range between 7.9 and 8.4 GHz. The conversion is achieved through double-conversion process which uses first and second local oscillator frequencies of 630-MHz and 7.2 to 7.7 GHz, respectively.

d. The 630-MHz local oscillator signal is generated by a voltage tuned oscillator in a phase locked loop which is controlled by a 10-MHz signal from the frequency synthesizer (not shown).

he second local oscillator signal is generated y a 1.

to 1.54-GHz microwave signal source which is phase locked to the 144 to 154-MHz signal from the frequency synthesizer to provide precise control and stability.

e. The 70-MHz input from the if patch panel above) is mixed with the first local oscillator frequency to produce a 700-MHz intermediate frequency (if.). The if signal is further processed and mixed with the second local oscillator frequency to produce an rf signal in the 7.9 to 8.4 MHz range. Three upconverter outputs are combined in a waveguide power combiner (not shown). The combined upconverter outputs are applied to traveling wavetube (twt) stage. The wt is operated just in saturation and provides he necessary drive power to the klystron power amplifier. A remotely controlled attenuator allows the terminal output to be adjusted downward from a maximum of 5 kilowatts (kW) at the antenna. The output from the klystron power amplifier is applied through protective circuitry not shown) to the antenna and is subsequently radiated to the satellite.

f. The return signal from the satellite is received at the antenna and is applied to the receiver section of the AN/TSC-54. The receive signal is applied through polarizers and duplexers (not shown), which provide 20 decibels (db) of isolation from the transmitter section to permit he use of one antenna, to an uncooled, low noise, three stage, parametric amplifier (LNA). The LNA provides 30 db of gain. The output of he LNA is applied to a low noise twt amplifier 7hich provides 29 db gain to signals in the 7.25 o 7.75-GHz range. The output of the twt amplifier is applied through a waveguide power divider (not shown) to three identical downconerters. The downconverters convert the 7.25 to .75-GHz receive signal into a 70-MHz if signal. : 'his conversion is achieved through a double-conversion process which uses first and second oscillator frequencies of 6.55 to 7.05-GHz and 30-MHz, respectively.

g. The first local oscillator signal is generated by using a 1.31 to 1.41-GHz microwave signal

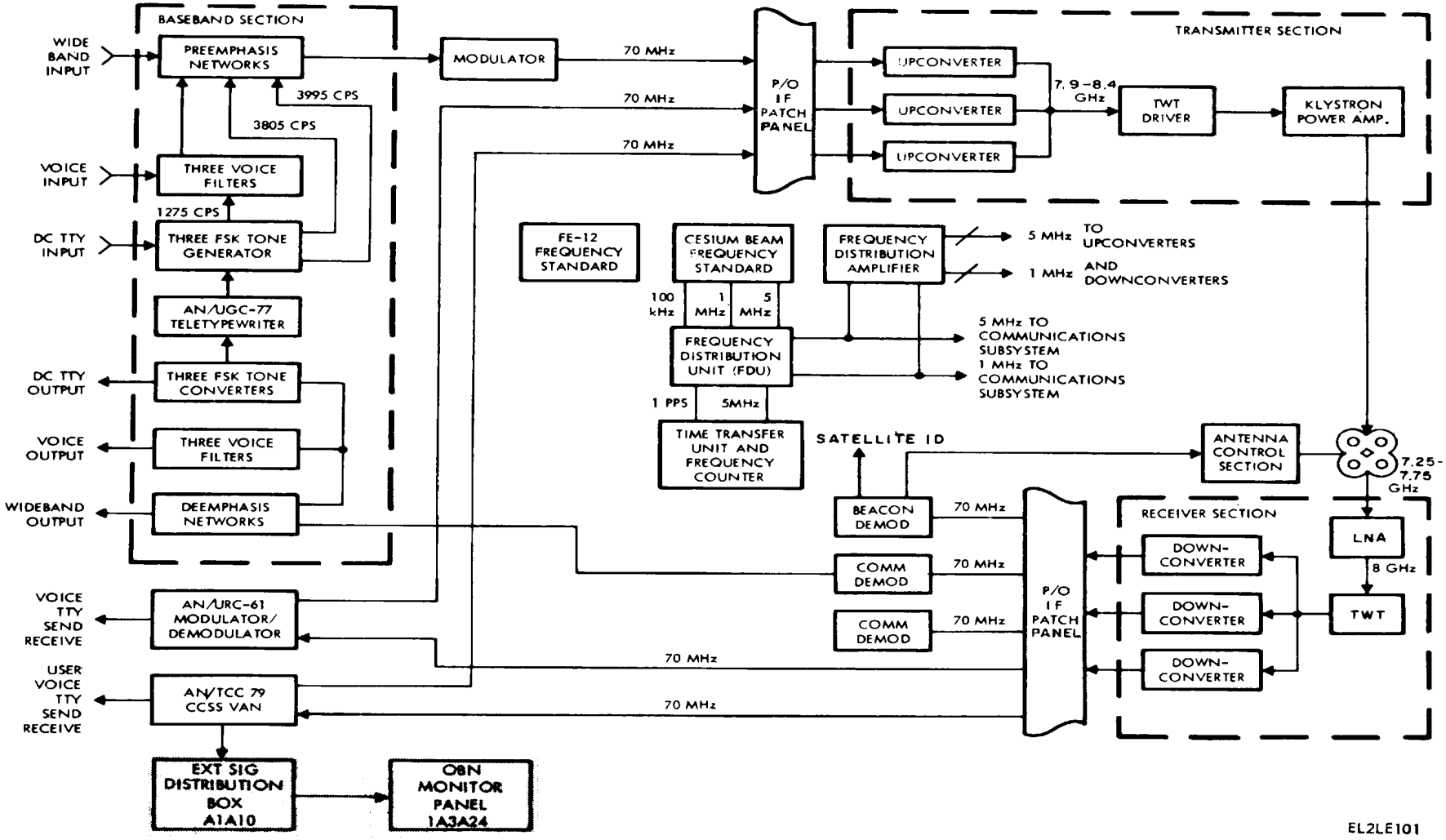

Figure 1-1. Satellite Communication Terminal AN/TSC-54, simplified block diagram.

source and a 5X frequency multiplier. The signal source is phase-locked to the 131 to 141-MHz signal from the frequency synthesizer (not shown). The second local oscillator signal is generated by using a voltage tuned oscillator which operates in a ease-locked loop controlled by the 10-MHz signal from the frequency synthesizer (not shown).

h. The 7.25 to 7.75-GHz signal from the power divider (f above) is mixed with the first local oscillator frequency to produce a 700-MHz if signal. The if signal is further processed and mixed with the second local oscillator frequency provide a 70-MHz signal to the if patch panel. The downconverters are capable of simultaneous downconversion of any three satellite frequencies. The signals at the if patch panel are available for application to two communication demodulators comm. demods), one beacon demodulator (beacon emod), and the AN/URC-61. In addition, AN/ CC-79 signals are routed through the if patch panel when used with the AN/TSC-54. Each FM demodulator of the AN/TCC-79 also sends an it-of-band noise (OBN) signal to the OBN monitoring panel to provide continuous indications of circuit quality for each FM channel.

i. The beacon demod has three selectable bandwidths to provide a normal, slightly improved, ad maximum acquisition sensitivity. The beacon emod applies an autotrack (error) to the antenna control section and satellite identification signal is available on the rear panel. The autotrack error signal enables position memory circuits within the antenna control section which allows the servo system to drive the antenna to the coordinates of he satellite. If the antenna does not lock on the satellite in four seconds the search process is repeated.

j. Each comm. demod (h above) demodulates he 70-MHz signal from the if patch panel and produces a composite signal containing voice and teletypewriter (tty) information which is applied o the deemphasis networks in the baseband section. The tty outputs from the deemphasis networks are applied through applicable fsk tone generators to the user and orderwire teletypewriters. The voice signal from the deemphasis networks is applied through one of three selectable filters to the user or orderwire handset.

1-9. Tabulated Data

Tabulated data applicable to the AN/TSC-54 is provided in TM 11-5895-389-12.

1-10. Reference Designations Cross References to Figure Numbers

To aid in the location of equipment shown on drawings, the reference designations are listed below along with the drawings on which they re shown.

Reference designation	*Equipment*	*Figure Fold Out*
1A2A1	Zero set control	2-3 sh 4, 2-3 sh 5, 2-8 sh 8, 2-9 sh 1.
1A2A44	Power distribution panel	2-6 sh 6, 2-7 sh 1, 2-7 sh 5, 2-7 sh 9, 2-8 sh 5, 2-8 sh 8, 2-9 sh 1.
1A2A5	Antenna control panel	2-3 sh 1, 2-3 sh 2, 2-3 sh 3, 2-3 sh 4, 2-3 sh 6, 2-3 sh 7, 2-3 sh 8, 2-3 sh 9, 2-6 sh 1, 2-6 sh 2, 2-6 sh 3, 2-6 sh 4, 2-6 sh 5, 2-7 sh 5, 2-7 sh 9, 2-8 sh 5, 2-8 sh 8, 2-9 sh 1.
1A2A9	Indicator panel	2-8 sh 8.
1A2A10	Link terminal timing central	2-7 sh 5, 2-7 sh 9, 2-8 sh 8.
1A2A21	Fan assembly	2-7 sh 9.
1A2A22	Frequency distribution unit	2-2 sh 19, 2-7 sh 5, 2-7 sh 9, 2-8 sh 8.
1A2A24	Cesium beam frequency standard	2-2 sh 19, 2-7 sh 5.
1A2A25	Cesium beam power supply	2-7 sh 5, 2-8 sh 8.
1A2A26	Test translator control	2-5 sh 2, 2-5 sh 3, 2-9 sh 1.
1A2A27	Power monitor and control	2-4 sh 1, 2-4 sh 2, 2-4 sh 6, 2-7 sh 5, 2-7 sh 9, 2-8 sh 5, 2-8 sh 8, 2-9 sh 1.
1A2A29	Time transfer unit	2-2 sh 19, 2-7 sh 5, 2-7 sh 9, 2-8 sh 8.
1A2A30/A31	Group delay equalizer	2-7 sh 5, 2-7 sh 9, 2-8 sh 8.

Reference designation	*Equipment*	*Figure Fold Out*
1A2A33	Distribution amplifier	2-2 sh 19, 2-7 sh 5, 2-7 sh 9, 2-8 sh 8.
1A2A34	Cesium environmental enclosure	2-7 sh 5, 2-7 sh 9.
1A2A35	Static frequency converter	2-7 sh 6, 2-7 sh 9.
1A3A3	Comm demod	2-1 sh 3, 2-2 sh 8, 2-2 sh 9, 2-2 sh 10, 2-3 sh 1, 2-5 sh 1, 2-5 sh 5, 2-8 sh 1, 2-8 sh 2, 2-8 sh 8, 2-9 sh 1.
1A3A4	Beacon demod	2-2 sh 11, 2-2 sh 12, 2-3 sh 1, 2-5 sh 6, 2-8 sh 8, 2-8 sh 10, 2-9 sh 1.
1A3A5	Comm demod	2-3 sh 1, 2-5 sh 5, 2-8 sh 3, 2-8 sh 8, 2-9 sh 1.
1A3A9	Comm demos PS	2-7 sh 6, 2-7 sh 9, 2-8 sh 1, 2-8 sh 2, 2-8 sh 3, 2-8 sh 8.
1A3A10	Beacon demod/ baseband PS	2-7 sh 6, 2-7 sh 9, 2-8 sh 2, 2-8 sh 3, 2-8 sh 4, 2-8 sh 8, 2-8 sh 10.
1A3A12	Baseband patch panel	2-1 sh 1, 2-1 sh 2, 2-1 sh 3, 2-1 sh 4, 2-1 sh 15, 2-1 sh 16, 2-2 sh 14, 2-2 sh 15, 2-2 sh 17, 2-2 sh 18, 2-2 sh 19, 2-8 sh 8.
1A3A13	Baseband control panel	2-1 sh 1, 2-1 sh 2, 2-1 sh 3, 2-1 sh 4, 2-2 sh 13, 2-2 sh 15, 2-2 sh 16, 2-2 sh 17, 2-2 sh 18, 2-2 sh 19, 2-8 sh 2, 2-8 sh 8.
1A3A14	Modulator	2-1 sh 7, 2-4 sh 7, 2-7 sh 6, 2-8 sh 8, 2-9 sh 1.
1A3A15	Baseband amplifier	2-1 sh 1, 2-1 sh 5, 2-1 sh 6, 2-2 sh 14, 2-2 sh 18, 2-8 sh 3, 2-8 sh 8, 2-9 sh 1.
1A3A16	Convertor-keyer echo suppressor	2-1 sh 3, 2-2 sh 16, 2-8 sh 4, 2-8 sh 8.
1A3A19	Fan control assembly	2-7 sh 6.
1A3A20	Fan assembly	2-7 sh 9.
1A3A22	If patch panel	2-1 sh 7, 2-1 sh 15, 2-2 sh 7, 2-2 sh 13.
1A3A23	Tty assembly	2-1 sh 2, 2-7 sh 6.
1A3A24	OBN monitor panel	2-2 sh 14.1, 2-9 sh 1.
1A3A25	Tty patch panel	2-1 sh 2, 2-1 sh 13, 2-1 sh 15, 2-2 sh 13, 2-2 sh 17, 2-8 sh 2.
1A3A26	LIU panel	2-1 sh 2, 2-2 sh 17, 2-7 sh 6, 2-7 sh 9, 2-8 sh 2.
1A4	Console base	2-1 sh 7, 2-1 sh 15, 2-1 sh 16, 2-2 sh 7, 2-2 sh 13, 2-2 sh 19, 2-5 sh 1, 2-7 sh 5, 2-7 sh 6, 2-7 sh 9, 2-8 sh 5, 2-8 sh 8, 2-9 sh 1.
1A9	Air conditioner filter asy	2-7 sh 4.
1A10	External signal distri-button box	2-1 sh 2, 2-1 sh 3, 2-1 sh 4, 2-1 sh 15, 2-1 sh 16, 2-2 sh 13, 2-2 sh 15, 2-2 sh 17.
1A12	Primary power distrib assy	2-7 sh 4, 2-7 sh 7, 2-7 sh 9.
1A13	Primary power filter	2-7 sh 4, 2-7 sh 9.
1A14	External power distribution box	2-8 sh 8.
1A15	Primary power distribution panel	2-7 sh 7, 2-7 sh 9, 2-8 sh 8.
1A17	Shelter heater	2-7 sh 7.

Reference designation	*Equipment*	*Figure Fold Out*
1A19	Freq conversion S/S	2-1 sh 8, 2-1 sh 9, 2-1 sh 10, 2-1 sh 11, 2-2 sh 5, 2-2 sh 6, 2-2 sh 7, 2-5 sh 4, 2-7 sh 7, 2-7 sh 9, 2-8 sh 8.
2A2	Power supply	2-4 sh 3, 2-4 sh 4, 2-8 sh 7, 2-8 sh 9.
2A3A3	Transmitter liquid cooler	2-4 sh 3, 2-7 sh 3, 2-7 sh 8, 2-9 sh 2, 2-10.
2A3A7	Transmitter control panel	2-1 sh 14, 2-4 sh 1, 2-4 sh 2, 2-4 sh 4, 2-1 sh 5, 2-4 sh 6, 2-7 sh 3, 2-7 sh 8, 2-8 sh 6, 2-8 sh 9, 2-9 sh 2.
2A3A9	Relay box assembly	2-4 sh 1, 2-4 sh 2, 2-4 sh 3, 2-4 sh 4, 2-4 sh 6, 2-7 sh 1, 2-7 sh 3, 2-7 sh 8, 2-8 sh 6, 2-8 sh 9, 2-9 sh 2.
2A3A10	Transmitter/exciter	2-1 sh 12, 2-1 sh 13, 2-1 sh 14, 2-4 sh 1, 2-4 sh 2, 2-4 sh 3, 2-4 sh 4, 2-4 sh 5, 2-4 sh 6, 2-7 sh 1, 2-7 sh 3, 2-7 sh 8, 2-8 sh 6, 2-8 sh 7, 2-8 sh 9, 2-9 sh 2, 2-10.
2A3A11	High voltage cage	2-4 sh 2, 2-4 sh 3, 2-4 sh 4, 2-7 sh 1, 2-7 sh 3, 2-7 sh 8, 2-8 sh 6, 2-8 sh 7, 2-8 sh 9, 2-9 sh 2.
2A3A14	Primary power distribution panel	2-1 sh 14, 2-3 sh 4, 2-3 sh 5, 2-3 sh 9, 2-4 sh 1, 2-4 sh 2, 2-4 sh 3, 2-4 sh 3, 2-4 sh 6, 2-6 sh 1, 2-6 sh 6, 2-7 sh 1, 2-7 sh 2, 2-7 sh 3, 2-7 sh 4, 2-7 sh 8, 2-8 sh 6, 2-8 sh 9, 2-9 sh 2, 2-12.
2A3A17	Servo amplifier	2-3 sh 9, 2-6 sh 6, 2-7 sh 3, 2-7 sh 8, 2-8 sh 9, 2-9 sh 2.
2A3A18	Servo amplifier	2-6 sh 6, 2-7 sh 3, 2-7 sh 8.
2A3A20	High voltage plate	2-4 sh 2, 2-4 sh 4, 2-7 sh 1, 2-7 sh 3, 2-8 sh 9.
2A3A21	Magnet power supply	2-8 sh 6, 2-8 sh 7.
2A3A22	Azimuth drive assembly	2-1 sh 14, 2-3 sh 4, 2-3 sh 5, 2-3 sh 9, 2-4 sh 1, 2-5 sh 2, 2-5 sh 3, 2-6 sh 1, 2-6 sh 6, 2-7 sh 2, 2-7 sh 3, 2-7 sh 8, 2-8 sh 7, 2-9 sh 2, 2-12.
2A3A23	Waveguide entrance	2-1 sh 11, 2-2 sh 7.
2A3A24	Intercom/Air monitor panel	2-8 sh 7, 2-12.
2A3PS1	Power supply	2-7 sh 2, 2-7 sh 8, 2-8 sh 6, 2-8 sh 9.
2A3PS2	Power supply	2-7 sh 2, 2-7 sh 8, 2-8 sh 6, 2-8 sh 9.
2A3PS3	Power supply	2-7 sh 2, 2-7 sh 8, 2-8 sh 7, 2-8 sh 9.
2A3PS4/PS5	Power supply	2-7 sh 1, 2-7 sh 8, 2-8 sh 7, 2-8 sh 9.
2A4	Mast	2-1 sh 14, 2-2 sh 1, 2-2 sh 7, 2-3 sh 3, 2-3 sh 5, 2-4 sh 1, 2-5 sh 2, 2-5 sh 3, 2-6 sh 6, 2-7 sh 8, 2-8 sh 7, 2-8 sh 9, 2-12.
2A4A3	Servo amplifier	2-3 sh 9, 2-6 sh 6, 2-7 sh 2, 2-7 sh 3, 2-8 sh 9.
2A4A4	Servo amplifier	2-3 sh 9, 2-6 sh 6, 2-7 sh 2.
2A4A6	Elevation data box synchro	2-6 sh 1, 2-9 sh 3.
2A4A9	Antenna	2-1 sh 14.

Reference designation	*Equipment*	*Figure Fold Out*
2A4B1	Drive motor	2-3 sh 9.
2A5	Elevation cable wrap	2-2 sh 7, 2-3 sh 3, 2-5 sh 2, 2-5 sh 3, 2-6 sh 1, 2-6 sh 6, 2-7 sh 2, 2-7 sh 8, 2-8 sh 7, 2-8 sh 9, 2-12.
2A9A1	Rf box	2-1 sh 1, 2-1 sh 2, 2-1 sh 3, 2-1 sh 4, 2-3 sh 3, 2-5 sh 2, 2-5 sh 3, 2-6 sh 6, 2-7 sh 2, 2-7 sh 8, 2-8 sh 7, 2-8 sh 9, 2-9 sh 3, 2-12.

CHAPTER 2
FUNCTIONING OF EQUIPMENT

Section I. INTRODUCTION

2-1. General

a. This chapter contains a functional diagram analysis of each major component of Satellite Communication Terminal AN/TSC-54. The functional diagrams illustrate signal, control, and power distribution paths within the AN/ TSC-54 from their points of origin to their points of termination (closed loop). The individual circuit paths are traced through units, modular assemblies, subassemblies, and circuit stages regardless of their physical location.

b. Circuit components (piece parts) are not shown on the functional diagrams except where they are necessary to clarify the action of a circuit upon a particular signal. Each function and operational characteristic of the individual components of the AN/TSC-54 is described in detail to provide a complete understanding of the operation of the equipment.

c. Many of the circuit stages in the AN/TSC54 are identical, differing only in reference designations of components parts. For purposes of this manual, only the transmitting, receiving, antenna positioning and control functions of the equipment are described. Detailed theory of the individual circuit stages within the block symbols shown on the functional diagrams, are covered in chapter 3.

d. Cross-reference to portions of multipart functional diagrams are made in the text to identify the point on the illustration at which the component and/or connections are made.

2-2. Types of Functional Diagrams

Three types of functional diagrams are used to describe the operational characteristics of the AN/TSC-54. The functional diagrams are contained in this manual.

a. Signal Flow Diagrams. Signal flow diagrams illustrate the circuit paths of transmitted, received, antenna positioning, and telephone signals throughout the AN/TSC-54. The individual circuit paths are essentially determined by the condition of the control circuits (*b* below) and other various operating conditions of the equipment. Secondary signal flow paths, such as indicating and monitoring functions, are also shown.

b. Control Circuit Diagrams. The control circuit diagrams illustrate the application of power to relay solenoids in accordance with specific operating conditions. The relays and associated contacts, in turn, result in an extended sequence of actions to control the circuit path to be taken by a given signal (a above).

c. Power Distribution Diagrams. The power distribution diagrams illustrate the power input circuits of each component of the AN/TSC-54 and show the complete distribution of alternating current (ac) and direct current (dc) voltages, grounds, and neutrals throughout the equipment, as required by the signal flow (*a* above) and control (*b* above) circuits to perform their proper functions.

2-3. Functional Diagram Characteristics

Symbology and other unusual characteristics of functional diagrams are described in a through j below:

a. Each console or cabinet, modular assembly, subassembly, or unit is identified by an enclosure represented by a dashed line in accordance with the physical breakdown of the equipment. A single dashed line indicates the overall unit or console. Two small dashes in the enclosure indicates the next largest subassembly, etc.

b. Official nomenclature, assigned names or references designations are used to identify all units, subassemblies, and modular assemblies of the AN/TSC-54 shown on the functional diagrams.

c. Circuit stages, other than amplifiers (*d* below), are shown as rectangular blocks.

d. Amplifier stages are represented by triangular blocks. The point of the triangle indicates the direction of signal flow.

e. Adjustable and variable components are represented by, their standard symbol and are shown with their assigned reference designation, name, or equipment panel marking. The

method of control (knob or screwdriver) is shown pictorially; screwdriver adjustments are represented by a slotted circle and knob controls are identified by the symbol of a selector knob.

f. Cross-reference between functions of the equipment and also between the various parts within a particular function are referenced at the outline or periphery of the equipment enclosure.

g. The functional nomenclature assigned to a circuit, stage, or assembly is descriptive and expressive as possible to establish a clear concept of the item to which it is assigned.

h. Equipment panel markings are capitalized in the text and blocked on the illustrations.

i. Broken lines indicate mechanical connections and solid lines indicate electrical connections.

j. The various abbreviations used for circuit and module identification are as follows:

(1) Baseband transformer line (BTL).
(2) Meter compensation network (MCN).
(3) Equalizing deemphasis network (EDN).
(4) Twin-tee network (TTN).
(5) Baseband transformer isolation (BTI).
(6) Baseband deemphasis network (BDN).
(7) Baseband preemphasis network (BPN).
(8) Baseband power amplifier (BPA).
(9) Baseband operational amplifier (BOA).
(10) Baseband differential amplifier (BDA).
(11) Baseband transformer setup (BTS).
(12) Baseband hybrid transformer (BHT).

Section II. TRANSMITTING FUNCTION

2-4. General

a. This section contains a functional analysis of the transmitting circuits of Satellite Communication Terminal AN/TSC-54. Basically, the terminal is capable of accepting voice, teletypewriter, and wideband multiplexed signals from an external line user, processing these signals and transmitting the signals by way of satellite to a compatible ground terminal. Simultaneously, a terminal orderwire, using an operating mode which does not conflict with the user, can transmit on the same radio frequency carrier within the range of 7.to 8.4 GHz.

b. A functional analysis of the baseband circuits is given in paragraphs 2-5 through 2-10 and paragraphs 2-11 and 2-12 cover the modulator amplifier circuits and operation of Radio Communications Subsystem AN/URC-61. A functional analysis of the rf components of the AN/TSC-54 is covered in paragraphs 2-13 through 2-17; the operation of fault and protective circuits is discussed in paragraphs 2-18 through 2-39.

2-5. Voice Signal Path

(fig. FO 2-1)

The transmitting circuits of the AN/TSC-54 provide one voice channel which can be assignee through landlines to an external user or an orderwire user (terminal user). For purposes of this manual, the user signal path is identified as user voice (a, b, and c below) and the orderwire user signal path is identified as orderwire voice (d through h below).

a. The user voice send signal (sheet 1) is applied to the AN/TSC-54 through USER-1SEND IN terminals El and E2 and fuses F1 and F2 to filter FL1 of the external signal distribution box 1A10. FL1 offers minimum attenuation to frequencies in the range of 0 to 4 kilohertz (kHz). The output of FL1 is applied through normalized-through USER VOICE NO. 1 EQUIP jacks J33 and J34, USER AMP LINE jacks J9 and J10, and fuses Fl and F2, to the primary winding of baseband line transformer T1. Line isolation is maintained by breakdown diodes CR1 and CR2 which prevent the voltage across the primary winding of T1 from exceeding 7.5 volts. Shunt resistor R35 limits the current flow through the primary winding.

b. The output from the secondary of T1 is applied as follows:

(1) Through SEND potentiometer R16B to baseland operational amplifier A17. SEND potentiometer R16B controls the gain of A17.

The output of A17 is applied through baseland operational amplifier A14 and baseland power amplifier A19 to the primary winding of baseland isolation transformer A33. Equalizing deemphasis network All, connected across A14, compensates for any signal envelope distortion.

(2) Through input meter calibrate potentiometer R1 and SEND-RECEIVE switch S1 to baseland operational amplifier A18 and also to meter compensation network A13.

NOTE

The metering circuits associated with the baseband transmitting function are covered in paragraph 2-9.

c. The nominal O dbm isolated user voice send signal from the secondary of baseband isolation transformer A33 is applied through normalized through USER AMP EQUIP jacks J31 and J32, on patch panel A3 of baseband patch panel 1A3A2, and VOICE SOURCE SEL SWITCH-

USER LINE jacks J7 and J8 to terminals 6 and 8 of VOICE lever switch S1 (sheet 2)

d. For two-wire user application, the hybrid user voice send/receive signal (sheet 1) is applied to the AN/TSC-54 through 2 WIRE-3-SEND/RCV terminals E5 and E6, and fuses F5 and F6 to filter FL3 of the external signal distribution box 1A10. FL3 also offers minimum attenuation to frequencies in the range of 0 to 4 kHz. The output of FL3 is applied through USER VOICE NO. 3 IN/OUT EQUIP jacks J35 and J36, HYBRID COIL 2W OUT/IN LINE jacks J11 and J12, and fuses F1 and F2 to the primary winding of baseband line transformer T1. Breakdown diodes CR1 and CR2 provide line isolation by preventing the voltage across the primary of T1 from exceeding 7.5 volts. The output from the secondary of T1 is applied to baseband hybrid transformer A15 and the outputs of the transformers are applied to HYBRID COIL LINE jacks J23 and J24 and MON jacks J71 and J72. HYBRID COIL LINE jacks J23 and J24 are patched to USER AMP LINE jacks J9 and J10 and the signal path from here on is the same as described in paragraphs *a* and *b* above.

NOTE

For receiving functions, the signal from HYBRID COIL IN EQUIP jacks J47 and J48 is applied in a reverse direction to the external user with the HYBRID COIL IN EQUIP jacks J47 and J48 patched to USER AMP LINE jacks J21 and J22 (FO 2-2, sheet 15).

e. The orderwire voice signal of the AN/TSC54 originates at handset assembly HS1 (sheet 1). When push-to-talk switch S1 is pressed, a circuit is completed from -28 vdc through resistor R30 to the handset transducer. The output of the transducer is applied across resistor R29 and ORDERWIRE AMPL SEND potentiometer R18B to baseband operational amplifier A52. Potentiometer R18B controls the gain of A52. The output of A52 is amplified by baseband power amplifier A57 and applied to meter calibrate potentiometer R5 and also through normalized-through ORDERWIRE AMP EQUIPMENT jacks J29 and J30 and VOICE SOURCE SEL SWITCH-O/W LINE jacks J5 and J6 to terminals 1 and 3 of VOICE lever switch S1 (sheet 2). The metering circuits used to monitor the orderwire voice signal are discussed in paragraph 2-9.

f. VOICE lever switch S1 is used to select the user voice signal (d above) or the orderwire voice signal (*e* above) for application (as the voice send signal) through normalized-through VOICE SOURCE SEL SW EQUIP jacks J27 and J28 (sheet 3) and ECHO SUPPR TRANSMIT LINE jacks J3 and J4 to echo suppressor transmitter A7. When operating with a two-wire user, the voice send signal is applied through the echo suppressor transmitter A7 to normalled-through ECHO SUPPR TRANSMIT EQUIP jacks J25 and J26 to DERIVATIVE CLIPPER MODE SEL jacks J1 and J2. When operating with a four-wire user, a patch cord is connected between VOICE SOURCE SEL SW EQUIP jacks J27 and J28 and DERIVATIVE CLIPPER MODE SEL LINE jacks J1 and J2 to disconnect the echo suppressor transmitter A7 from the signal path. The voice send signal from DERIVATIVE CLIPPER MODE SEL LINE jacks J1 and J2 is applied to terminals 3 and 6 of CLIPPER lever switch S2 (sheet 4).

g. When CLIPPER lever switch S2 is set to IN, terminal 6 is grounded and the voice send signal present at terminal 3 is applied to baseband operational amplifier A8. The voice send signal is amplified and clipped by baseband operational amplifiers A8 and A3. During the absence of a voice send signal, baseband operational amplifier A8 receives a 10-kHz squelch signal from a 10-kHz oscillator circuit comprised of baseband operational amplifier A7 and twin-tee network and level control A6. The output of the 10-kHz oscillator circuit is developed across derivative clipper threshold adjust potentiometer R5. Potentiometer R5 is used to adjust the amplitude of the 10-kHz input signal to baseband operational amplifier A8. During the absence of a voice input signal, the 10-kHz squelch signal is amplified and clipped by baseband operational amplifiers A8 and A3 to prevent system noise from being amplified and applied to baseband power amplifier A2. The voice send signal is amplified by baseband power amplifier A2 and is then applied through baseband isolation transformer A1 to terminals 7 and 10 of CLIPPER lever switch S2.

h. The voice send signal (g above) is applied through closed contacts 7 and 9 and 10 and 12 of CLIPPER lever switch S2 to terminals 4 and 10 of MODE SELECT switch S5A. With CLIPPER lever switch S2 is set to OUT, the voice send signal bypasses the clipper circuits.

(1) When MODE SELECT switch S5 is set to V1, the voice send signal is applied to VOICE/ TTY FIL TP LINE jacks J1 and J2 on patch panel A2 of baseband patch panel 1A3A2 and through voice/tty filter FL5 to terminals 2 and 8 of switch S5B. VOICE/TTY FIL TP LINE jacks J1 and J2 are used to monitor the voice send signal input to filter FL5 which is a notch type

filter consisting of two sections; a band stop section and a bandpass section. The band stop section passes frequencies in the range of 300 to 1, 180 Hz and 1,370 to 3,500 Hz and offers greater than 60 db rejection to frequencies in the range of 1,180 to 1,370 Hz. The bandpass section passes frequencies in the range from 1,180 Hz to 1,370 Hz and offers greater than 60 db rejection to all other frequencies. This allows the last ditch 1,275 Hz signal to be placed within the voice baseband without interfering with the voice signal. The output of FL5 is applied to terminals 2 and 8 of MODE SELECT switch S5B and to VOICE/TTY FIL LINE EQUIP jacks J25 and J26 and MON jacks J49 and J50 which provide monitoring points for the output of FL5. The signal path from MODE SELECT switch S5 is covered in paragraph 2-7.

(2) When MODE SELECT switch S5 is set to the V2 position, the voice send signal is applied to terminals 1 and 2 of truncated filter FL3 and to TRUNCATED FIL LINE jacks J3 and J4. TRUNCATED FIL LINE jacks J3 and J4 are used to monitor the voice input signal to FL3 which passes only voice frequencies in the range of 300 to 1,800 Hz. The voice output signal from truncated filter FL3 is applied to contacts 3 and 9 of MODE SELECT switch S5B and to TRUNCATED FIL EQUIP jacks J27 and J28 and MON jacks J51 and J52 which provide the monitoring points for the output of filter FL3.

(3) When MODE SELECT switch S5 is set to V3, the voice signal is applied to terminals 1 and 2 of normal filter FL1 and to NORMAL FIL LINE jacks J5 and J6. NORMAL FIL LINE jacks J5 and J6 are used to monitor the voice input signal. Filter FL1 passes voice frequencies in the range of 300 to 3,400 Hz and the voice output signal of FL1 is applied to contacts 4 and 10 of switch S5B and to NORMAL FIL EQUIP jacks J29 and J30 and MON jacks J53 and J54 which are used to monitor the output voice signal of filter FL1.

2-6. Teletypewriter Signal Paths (fig. FO 2-1)

The AN/TSC-54 provides one teletypewriter (tty) channel for an external user through landlines and one tty channel for an orderwire user. For purposes of this manual, the external user tty signal is identified as user tty (a and b below) and the orderwire user tty signal is identified as orderwire tty (c and d below). Either the external user or orderwire user may also operate in the last ditch mode (c below).

a. The user tty input signal (sheet 2) is applied to the AN/TSC-54 through LIU-1 SEND IN terminals E65 and E66 and fuses F65 and F66 to filter FL33 of external signal distribution box 1A10. Filter FL33 passes frequencies in the range of 0 to 4 kHz. The output of filter FL33 is applied through J2 pins *A* and *B* of the line isolator A1 of line isolation unit 1A3A26, A1 provides isolation between the out-station and in-station signals. A1 also converts the user tty signal to a standard polar $\pm$6 volt signal which is applied from J3 pins *D* and *E* on the line isolation unit to TX LIU-1 3995 Hz USER EQUIP jack J1B and MON jack J27 on the tty patch panel 1A3A25. EQUIP jack J1B is normalized through to the TTY SEL SW 3995 Hz TX LINE jack J1A. The user tty signal at LINE jack J1A is applied to contacts 7 and 9 of the TTY MODE USER lever switch S4 of baseband control panel 1A3A13. With TTY MODE USER lever switch S4 set to NORMAL, contacts 7 and 8, and 9 and 10 (S4-L) are made and the user tty signal is applied to pins 5, 6, and 16 of the 3995-Hz frequency shift keyer A3 of converter-keyer-echo suppressor 1A3A16 (sheet 3). With the TTY MODE USER lever switch S4 (sheet 2) set to NORMAL, contact 11 and 12 also make and disable the 1275-Hz frequency shift keyer A1 of converter-keyer-echo suppressor 1A3A16 (sheet 3) by completing a ground loop that shorts pins 4 and 14 to inhibit the generation of the 1275-Hz tone. The 3995-Hz frequency shift keyer A3 converts the user dc tty signal to mark and space outputs which are applied from pins 22 and 23 on the frequency shift keyer A3 to the 3995 C/S KEYER EQUIP jacks J31 and J32, and MON jacks J55 and J56 on patch panel A1 of baseband patch panel 1A3A12. The 3995 C/S KEYER EQUIP jacks J31 and J32 are normalized through to COMM AMPL 3995 C/S LINE jacks J7 and J8 to the baseband differential amplifier A5 of baseband amplifier 1A3A15 (sheet 5). The output of differential amplifier A5 is developed across 3995 level adjust potentiometer R22A.. The signal at the wiper arm of potentiometer R22A is amplified by baseband operational amplifier A10 and applied as follows:

(1) Through contact C1 of EMPHASIS SELECT switch S7 to the appropriate preemphasis and deemphasis network.

(2) Through meter calibrate resistor R7 (sheet 6) to the metering circuits associated with the baseband function.

b. The orderwire tty signal (sheet 2) is applied to LIU-2-SEND IN terminals E69 and E70, and Fuses F69 and F70 to filter FL35 of external signal distribution box 1A10. Filter FL35 passes frequencies in the range of 0 to 4 kHz. The output of filter FL35 is applied through J2 pins u

and *v* to line isolator A2 of line isolation unit 1A3A26. A2 functions in a manner identical to A1 described in a above. The output of A2 is applied from J3 pins X and Y on the line isolation unit to TX LIU-2 3805 Hz OW EQUIP jack J3B and MON jack J29 on the tty patch panel 1A3A25. EQUIP jack J3B which is normalized through to the TTY SEL SW 3805 Hz TX LINE jack J3A applies the signal to contacts 7 and 9 of TTY MODE ORDERWIRE lever switch S3 of baseband control panel 1A3A13. With TTY MODE ORDERWIRE lever switch S3 set to NORMAL, contact 7 and 8, and 9 and 10 (S3-L) are made, and the orderwire tty signal is applied to pins 5, 6, and 16 of the 3805-Hz frequency shift keyer A2 of converter-keyer-echo suppressor 1A3A16. With TTY MODE ORDERWIRE lever switch S3 (sheet 2) set to NORMAL, contacts 11 and 12 (S3-L) also make and disable the 1275-Hz frequency shift keyer A1 of converter-keyer-echo suppressor 1A3A16 (sheet 3) to inhibit the generation of the 1275-Hz tone. The 3805-Hz frequency shift keyer A2 converts the dc orderwire tty signal to mark and space frequency outputs which are applied to the 3805 C/S keyer EQUIP jacks J33 and J34 and MON jacks J57 and J58 on patch panel A1 of baseband patch panel 1A3A12. EQUIP jacks J33 and J34 are normalized-through to COMM AMPL 3805 C/S LINE jacks J9 and J10 to baseband differential amplifier A3 of baseband• amplifier 1A3A15 (sheet 5). The output of baseband differential amplifier A3 is developed across 3805 level adjust potentiometer R21A and is amplified by baseband operational amplifier A4 and applied as follows:

(1) Through contact C1 of EMPHASIS SELECT switch S7 to the appropriate preemphasis and deemphasis network.

(2) Through meter calibrate resistor R8 (sheet 6) to the metering circuits associated with the orderwire tty signal.

NOTE

The send signal from connector J2 pins A and B on the UGC-77 teletypewriter assembly 1A3A23 (sheet 2), is applied to TX UGC-77 KEYER PTR EQUIP jack J9B and MON jack J35 on the tty patch panel 1A3A25. In the event the UGC-77 is to be used as the orderwire user, EQUIP jack J9B must be patched to TTY SEL SW 3805 TX LINE jack J3A.

c. The last ditch tty send mode may be used for a user tty input (a above) or the orderwire tty input (b above). When either a user tty input or the orderwire input is selected for last ditch operation, the associated frequency shift keyer is disabled and the 1275-Hz frequency shift keyer is enabled.

(1) When TTY MODE USER lever switch S4 of baseband control panel 1A3A13 (sheet 2) is set to LAST DITCH, a ground loop is completed through contacts 3 and 4 of switch S4 (S4-R) disabling the 3995-Hz frequency shift keyer A3 of converter-keyer-echo suppressor 1A3A16 (sheet 3). The 1275-Hz frequency shift keyer, of 1A3A16, is enabled by open contacts 11 and 12 of switch S4 (S4-L) and the dc input to the 3995-Hz frequency shift keyer A3 is opened by contacts 7 and 8. With TTY MODE USER switch S4 (sheet 2) set to LAST DITCH, contacts 1 and 2, and 5 and 6 are also made, which applied the user tty signal to TX TTY SEL SW 1275 Hz L/D EQUIP jack J7B and MON jack J33 on the tty patch panel 1A3A25 (sheet 3). EQUIP jack J7B is normalized-through to KEYER CONV 1275 Hz TX LINE jack J7A. The user tty signal at J7A is applied to pins 5, 6, and 16 of the 1275-Hz frequency shift keyer A1 of converter-keyer-echo suppressor 1A3A16. The output signal at pins 22 and 23 of the 1275-Hz frequency shift keyer A1 is applied to the 1275 C/S KEYER EQUIP jacks J35 and J36, and MON jacks J59 and J60 on patch panel A1 of baseband patch panel 1A3A12.
EQUIP jacks J35 and J36 are normalized through to VOICE/TTY TG LINE jacks J11 and J12. The signal at LINE jacks J11 and J12 is applied through pins *f* and *g* of connector P32, to pins 3 and 4 of voice/tty filter A17FL5 of baseband control panel 1A3A13 (sheet 4). The output of A17FL5 is identical to that discussed in paragraph 2-5*h*(1).

(2) When TTY MODE ORDERWIRE switch S3 of baseband control panel 1A3A13 (sheet 2) is set to LAST DITCH, a ground loop is completed through contacts 5 and 6 of switch S3 (S3-R) to disable the 3805-Hz frequency shift keyer A2 of converter-keyer-echo suppressor 1A3A16 (sheet 3). The 1275-Hz frequency shift keyer 1A, of 1A3A16, is enabled by opening contacts 11 and 12 of switch S3 (S3-L) and the dc input path of the 3805-Hz frequency shift keyer A2 is opened by contacts 9 and 10. With TTY MODE ORDERWIRE switch S3 (sheet 2) set to LAST DITCH, contacts 9 and 10. With TTY MODE ORDERWIRE switch S3 (sheet 2) set to LAST DITCH, contacts 1, 2, 3, and 4 (S3-L) are made and apply the orderwire tty signal to TX TTY SEL SW 1275 Hz L/D EQUIP jack J7B and MON jack J33 on the tty patch panel 1A3A25 (sheet 3).
The signal path from EQUIP jack J7B is identical to the user tty signal path discussed in (1) above.

2-7. Wideband Multiplex Signal (Transmit

(fig. FO 2-1, sheet 4)

The wideband multiplex send signal is applied the AN/TSC-54 through wideband external input jack J4 and fuses F101 and F102, of t external signal distribution box 1A10, normalized-through WIDEBAND EXT EQU jacks J31 and J32, MON jacks J55 and J56, a VOICE MODE SEL SW WIDEBAND LIE jacks J7 and J8 on patch panel A2 of baseband patch panel 1A3A12, and then through baseband isolation transformer A17A9 to contacts 6 and 12 of MODE SELECT switch S5B baseband control panel 1A3A13. When t MODE SELECT switch is set to V5, the wideband multiplex signal is selected as discussed paragraph 2-8.

2-8. Composite Voice and Teletypewriter Signal

(fig. FO 2-1)

a. The following modes of operation can selected with MODE SELECT switch S5 baseband control panel 1A3A13 (sheet 4):

(1) Position V1 selects the output of vc tty filter A17A5 which consists of voice frequencies in the range of 300 to 1,180 Hz, 1,370 to 3,1 Hz, and the last ditch tty frequency of 1,275 I

(2) Position V2 selects the output of truncated filter A17FL3 which consists of voice frequencies in the range of 300 to 1,800 Hz.

(3) Position V3 selects the 300 to 3,400 voice frequency output of normal filter A17F

(4) Position V4 is not connected.

(5) Position V5 selects the 0 to 23 kHz multiplex wideband signal.

b. The composite voice/tty signal (0 dbm level is applied from contacts C1 and C2 of MO] SELECT switch S5B, normalized-through VOICE MODE SEL SW EQUIP jacks S29 a J30, MON jacks J53 and J54, and COMM AM VOICE LINE jacks J5 and J6 to baseband differential amplifier A1 (sheet 5). The amplified o put of baseband differential amplifier A1 is developed across VOICE potentiometer R20A. signal at the wiper arm of potentiometer R2 is amplified by baseband operational amplilfierA6 and applied as follows:

(1) Through contact C1 of EMPHASIS SELECT switch S7 to the appropriate preemphasis and deemphasis network.

(2) Through meter calibrate potentiometer 1A3A15R9 (sheet 6) to the associated meter circuits.

c. The user tty 3995-Hz fsk signal, the orderwire tty 3805-Hz fsk signal, and the composite, voice/tty signals are combined at EMPHASIS SELECT control switch 1A3A15S7 (sheet 5) to complete the baseband frequency composition. The selected preemphasis network accentuates the higher baseband frequencies to improve the signal-to-noise ratio when the signal is used to modulate the carrier frequency. The output of he selected preemphasis network is applied to COMP potentiometer R23 which is used to adjust the amplitude of the input signal applied to baseband power amplifier 1A3A15A1A8 (sheet 6). The amplified output of baseband power n amplifier A8 is applied through contacts 1 and 3 of armature relay A12 to meter calibrate potentiometer R10 and through pin J of connector J1 n to normalized-through COMM AMPL EQUIP jacks J25 and J26, MON jacks J49 and J50, and MODULATOR LINE jacks J1 and J2. The baseband signal from LINE jacks J1 and J2 is 9' applied to modulation amplifier A1 in modulator 1A3A14 (sheet 7) (para 2-11).

2-9. Baseband Metering Circuit

(fig. FO 2-1)

The metering circuits associated with the baseband send function are discussed in a through d below:

a. USER LINE AMPL LEVEL meter 1A3A15M1 (LEVEL-meter M1) (sheet 1) and its associated circuit .components are used to monitor the user voice input and user voice output signals of baseband amplifier A15. When USER LINE AMPL SEND-RECEIVE control switch S1 (SEND-RECEIVE control switch S1) is set to SEND IN, the input signal, developed across meter calibrate potentiometer R1, is applied through baseband operational amplifier A18 and meter compensation network A13 to LEVEL meter M1. With SEND-RECEIVE control switch S1 set to SEND OUT, the output signal developed across meter calibrate potentiometer R2 is applied to LEVEL meter M1. Meter compensation network A13 provides protection for the meter by ensuring that the output signal applied does not exceed a safe level; it also provides a small deflection voltage to deflect the pointer to the first meter division on the scale, thus ensuring that the meter pointer is not resting against a stop when the input signal is received. Meter calibrate potentiometers R1 and R2 are adjusted for a zero meter , indication with a 0-dbm input signal to baseband amplifier A15.

b. Vu LEVEL meter M2 and its associated circuit components are used to monitor the orderwire voice input to baseband amplifier A15. With SEND-RECEIVE switch S2 set to SEND,

the orderwire voice signal, developed across meter calibrate resistor R5 is applied to baseband operational amplifier A53. The amplified output signal is applied through meter compensation network A58 to LEVEL meter M2. The compensation network is provided so that identical meters can be used in various circuits and can be calibrated to indicate 0 vu over a wide range of input signal levels. The meter compensation network also insures that the output to the meter does not exceed a safe level Meter calibrate potentiometer R5 is adjusted for a zero meter indication when the input signal level is known to be correct. c. Vu SEND LINE AMPL meter M4 (sheet 6: and its associated circuit components are used to monitor the baseband voice, 3805 teletypewriter, 3995 teletypewriter, and the composite baseband signals. SEND LINE AMPL selector switch S4 receives all the signals to be monitored from the wiper arms of meter calibrate potentiometers R7 through R10 and applies the selected signal to baseband operational amplifier A24. The signal is amplified by baseband operational amplifiers A24 and A30 and applied through meter compensation network A28 to Vu SEND LINE AMPL meter M4. The compensation network provides compensation so that identical meters can be used in various circuits and can be calibrated to indicate 0 vu over a wide range of input signals levels; it also provides protection by ensuring that the output signal to the meter does not exceed a safe level.

d. VOLTMETER M2 (sheet 3) on the baseband control panel is used to monitor dc tty signal voltages. In order to monitor these voltages, a patch must be made on the tty patch panel 1A3A25 between +6V METER jack (J76) and the monitor jack corresponding to the tty channel of interest.

e. LOOP CURRENT meter M1 is used to monitor user high level tty loop currents on the out-station side of the line isolation units. In order to monitor user out-station signals, a patch must be made from the MONITOR INPUT jack (J10) on the baseband control panel 1A3A13 to the user side of the appropriate line isolation unit (LIU).

2-10. Test Tone Generation

(fig. FO 2-1, sheet 6)

a. The 1-kHz test tone generation circuits produce a calibrated (O dbm at 1 kHz) and uncalibrated output which are used for test purposes. Baseband operational amplifier A35 and twin-tee network and level control A34 comprise a l-kHz oscillator. The l-kHz output at pin 2-5 of operational amplifier A35 is applied to the junction of level adjust potentiometers R15 and R28. Potentiometer R15 is used to adjust the test tone of baseband power amplifier A38 for O dbm. (1) When MAN-PRESET level switch S8 is set to PRESET and ON-OFF-MC lever switch S5 is set to ON, the 1-kHz test tone is applied from the wiper arm of potentiometer R15 through MAN-PRESET lever switch S8 to baseband tone filter A39. The 1-kHz test tone output at pins 1-2 and 1-3 of baseband tone filter A39 is amplified by baseband operational amplifiers A40 and A38. The output from pin 1-10 of operational amplifier A40 is applied to pin 1-10 of the baseband tone filter as a feedback signal. The calibrated 0-dbm 1-kHz output. of baseband power amplifier A38 is applied to contact 6 of armature relay A12 and to normalized-through 1 KC TEST TONE EQUIP jacks J27 and J28 and MON jacks J51 and J52. A ground is applied through contacts 2 and 1 of ON-OFF-MC lever switch S5 to illuminate TONE indicator DS2.

(2) When SEND LINE AMPL selector switch S4 is set to COMP, a ground is also applied through contacts 3 and 4 of switch S5 to energize relay A12. This selects the 1-kHz test tone as the output in place of the composite baseband output.

b. When MAN PRESET lever switch S8 is set to MAN and ON-OFF-MC lever switch S5 is set to ON, the output level of baseband power amplifier A38 is uncalibrated and is controlled by the setting of potentiometer R28. UNCAL indicator DS1 is illuminated by the application of +28 volts through contacts 4 and 5 of switch S8 and a ground that is applied through contacts 1 and 2 and 3 and 4 of switch S5.

(1) When ON-OFF-MC lever switch S5 is set to OFF, the 1-kHz tone is inhibited by a ground applied through contacts 4 and 3 and 2 and 1 of switch S5 to pin 2-1 of baseband tone filter A39.

(2) When ON-OFF-MC level switch S5 is set to MC (momentary contact), the ground for indicator lamps DS1 and DS2 is applied through contacts 6 and 5 and 7 and 8 of switch S5 and the disabling ground at pin 2-1 of tone filter A39 is removed by open contacts 3 and 4.

2-11. Modulator Amplifier Circuits

(fig. FO 2-1, sheet 7 and fig. FO 2-4, sheet 7)

a. The baseband input signal (para 2-8) is coupled through transformer T1 to a resistive network matrix module and dc amplifier. DEVIATION CONTROL PRESET MODE selector switch, and MANUAL ADJUST 10 DB control

switches are used to control the output level of dc amplifier AR1. Operation of the switches and matrix module is discussed in f below. The amplified baseband output of dc amplifier AR1 is applied to potentiometer R3 which is used to adjust the input level to dc amplifier AR1 in phase lock loop amplifier A9. The second input to dc amplifier AR1 is from the phase lock loop circuits (*b* below). The amplified baseband output signal from dc amplifier AR1 is applied to 10-MHz uco A3 and to frequency deviation monitor A2. The baseband signal frequency modulates the output of 10-MHz uco A3 and the modulated output is applied to X7 frequency multiplier A6. The frequency modulated 10-MHz signal is multiplied seven times and applied through 70-MHz bandpass filter A5 to if patch panel A22. The bandpass filter has a bandwidth of 1.4 MHz centered at 70 MHz to reject any spurious harmonics. A second output of the bandpass filter is applied to level detector and fault lamp driver A8. The modulator signal is applied through power divider DC1, fixed attenuator (AT1) and modulator jack coupler CP4 on the if patch panel A22. Coupler CP4 makes the 70-MHz modulator signal available for patching to the appropriate upconverter jack. Power divider DC1 also supplies a sample of the signal to mod test jack coupler CP5. Except during modulator test, coaxial termination (AT5) absorbs the signal sample. The power amplification process of the 70-MHz modulator output is covered in paragraph 2-14.

b. The 10 MHz uco is phase locked to the 100 kHz frequency standard input from the distribution amplifier by the phase lock loop circuits. The 100-kHz reference frequency at a level of +6 dbm is applied through 10-db attenuator AT1 to ÷100 frequency and phase detector A7. The output of uco A3 is applied to ÷100 countdown module AR1. The vco output is counted down by a factor of 100: 1 and the output signal is applied to 100 kHz phase detector AR2. Phase detector AR2 compares the signal from ÷100 countdown module AR1 with a 100 kHz reference input signal and detects any phase (frequency) difference. The detected phase error signal is applied to 100-kHz detectors AR3 and AR4. The dc phase error signal output of detector AR4 is amplified by dc amplifier AR5 and applied through a low pass filter to dc amplifier AR1 in phase lock loop amplifier A9. The polarity of the dc phase error voltage is determined by the direction of frequency error (above or below 10 MHz) of the vco. The error voltage is applied to the uco as a dc correction voltage to return the vco output to 10 MHz.

c. Level detector AR2 and its associated circuit components in phase lock loop amplifier A9 comprise a false lock detect circuit to prevent false lock-on form spurious signals. During power turn-on, any spurious output from -100 frequency and phase detector A7 is integrated and amplified by AR2. If the spurious output is of sufficient amplitude to cause a false lock-on condition, the output of AR2 disables the 100 kHz phase detector and allows the 10 MHz uco time to stabilize at 10 MHz. With the spurious signals removed from the input to AR2, the charge across the associated integrator network decays and the disable voltage is removed from the 100 kHz phase detector to allow the phase lock loop circuit to function normally.

d. The modulator circuits of the AN/TSC-54 provide the following front panel monitoring indications: 100 KC REF, ÷100, 0 LOCK. 10 MC VCO, and 70 MC OUTPUT. The 100 kc detector AR3 provides an output to level detector AR1. If the amplitude of the 100 kHz reference signal is normal, level detector AR1 produces a negative output to disable the lamp driver amplifier. With the lamp driver disabled, 100 KC REF indicator lamp DS2 is extinguished. If the 100 kHz fault signal decreases below the threshold point of level detector AR1, the level detector is cutoff and the positive output initiates the lamp driver - amplifier, illuminating 100 KC REF indicator lamp DS2. The remaining four fault circuits function the same as the 100 kHz fault circuit except for the signal input.

e. Deviation monitor A2 and frequency DEVIATION meter M1 provide the peak deviation indication of the 70-MHz rf carrier output of the modulator by monitoring the amplitude of the baseband modulating signal. Since the rf deviation is proportional to the amplitude of the modulating signal, meter M1 can be calibrated in terms of frequency deviation. The baseband signal from dc amplifier AR1 in phase lock loop amplifier A9 is applied to deviation monitor A2 where it is amplified and peak detected. Frequency meter selector switch S1 has three positions, 6 KC, 60 KC, and 600 KC, which provide meter M1 with three different full scale ranges.

f. The matrix module (*a* above) is illustrated in figure FO 2-4, sheet 7 and is used to preset the gain of dc amplifier AR1 for twelve selectable modes of operation. The voltage divider comprised of resistors R1 through R10 divide the input signal from transformer T1 into eight signal levels, in 10 db increments, which are applied to the matrix module. The matrix module has twelve lines which cross the eight input level lines. These twelve lines represent position

V1 through V12 of DEVIATION CONTROL PRESENT MODE selector switch S2A. By inserting a plug into the hole where the input level lines and the mode lines cross each other, any one of the eight input levels can be connected to any one of the twelve positions, and the selected signal level is applied to amplifier AR1. The voltage divider comprised of resistors R16 through R26 divides the output amplifier AR1 into eleven discrete 1 db steps which are applied to the matrix module. The matrix module has twelve lines which cross the eleven input level lines and these twelve lines represent positions V1 through V12 of DEVIATION CONTROL PRESET MODE selector switch S2B. By inserting a plug into the hole where the input level lines cross the mode lines, any one of the eleven input steps can be connected to any one of the twelve positions of the switch. The selected signal level is applied as negative feedback, through capacitor C1, to the input of modulation amplifier AR1. By setting the input signal level to modulation amplifier AR1 in 10 db steps and setting the amount of feedback in 1 db steps, each selected output of modulation amplifier AR1 can be preset to any level between -50 db to +20 db in 1-db steps. When selector switch S2 is set to MANUAL ADJUST, section A is connected to the output of MANUAL ADJUST 10 DB switch S4 and section B is connected to the output of MANUAL ADJUST 1 DB switch S3. Under this condition the matrix module is bypassed and switch S4 is used to select one of the eight levels from the R1 through R10 voltage divider and switch S3 is used to select one of the eleven levels from the R16 through R26 voltage divider. The output of each switch is applied through the MANUAL ADJUST position of selector switch S2 to dc amplifier AR1.

2-12. Radio Communications Subsystem AN/URC-61

(fig. FO 2-1)

a. The user tty signal (sheet 3) is applied through URC-61 DC USER SEND IN terminals E85 and E86 and fuses F85 and F86 to the teletypewriter patch panel 1A3A25. At the teletypewriter patch panel, the user tty signal is applied through normalized-through TX URC-61 USER EQUIP jack J13B, MON jack J39 and TX URC-61 USER LINE jack J13A to the URC-61.

b. The orderwire tty signal is applied through URC-61 DC OW SEND IN terminals E81 and E82 and fuses F81 and F82 to the teletypewriter patch panel. At the teletypewriter patch panel the orderwire tty signal is applied through normalized-through TX URC-61 OW EQUIP jack J11B, MON jack J37 and TX URC-61 OW LINE jack J11A to the URC-61.

c. The AN/URC-61 user voice signal (sheet 15) is applied through URC-61 SEND 4 terminals E7 and E8 and fuses F7 and F8 to filter FL4. The user voice output is applied to the vf baseband patch panel 1A3A12A4. At the vf baseband patch panel, the user voice is applied through normalized-through USER VOICE NO. 4 EQUIP jacks J25 and J26, MON jacks J49 and J59, and URC-61 VOICE LINE jacks J1 and J2 to connector J2 on the AN/URC-61.

d. The user digital data is applied through DIG DATA SEND IN terminals E89 and E90 and fuses F89 and F90 to the teletypewriter patch panel 1A3A25. At the teletypewriter patch panel, the digital data signal is applied through normalized-through TX URC-61 DIG DATA EQUIP jack J15B, MON jack J41, and URC-61 DIG DATA TX LINE jack J15A to connector J2 on AN/URC-61.

e. The user inputs to the AN/URC-61 (*a* and *b* above) are used to modulate a 70-MHz carrier and the modulated 70 MHz is applied from connector J7 on the AN/URC-61 to URC-61 coupler CP3 on AN/TSC-54 if patch panel. At the patch panel, the signal is normally routed through the group delay equalizer couplers CP2 and CP9 to the appropriate upconverter jack.

2-13. Frequency Upconversion

(fig. FO 2-1)

a. The frequency modulated (fm) send signals from the communications patching panel are converted to discrete transmit frequencies by three identical upconverters. Each upconverter converts a 70-MHz $\pm$20-MHz if signal into an rf signal in the frequency range between 7.9 to 8.4 GHz.

b. The 70-MHz if signal (sheet 10) is applied to the upconverter through step attenuator A2. Step attenuator A2 provides 0 -to 21-db attenuation in one db step to compensate for input signal levels between -10 and + 10 dbm.

c. From step attenuator A2, the 70-MHz if signal is applied to phase equalizer EQ1 and amplitude attenuator AT9 through directional coupler DC1. Equalizer EQ1 and attenuator AT9 compensate for the phase and amplitude characteristics of the following circuitry. Directional coupler DC1 provides an isolated 70-MHz signal sample for application to amplifier A9 and detector A10. The amplifier and detector units monitor the signal sample and provide a dc voltage which is proportional to the signal level.

This voltage is applied to STATUS meter M1 through status indicator calibration unit A6 and STATUS switch S1 for monitoring purposes.

d. The 70-MHz output of amplitude attenuator AT9 (c above) is applied to the if conversion assembly CR1 where it is mixed with the 630-MHz local oscillator signal from if phase-locked oscillator Y2. The resulting 700-MHz if signal is applied to the if circuit for further processing. The if conversion assembly CR1 also provides a 630-MHz local oscillator test output and a dc voltage which is proportional to the local oscillator input power level. The test output is routed to front panel IF LO SAMPLE connector J5. The dc voltage is applied to meter M1 through status indicator calibration unit A6 and switch S1. Termination AT3 provides 50 ohm terminatttttttitiitiimpedance for J5 when it is not in use.

e. The 630-MHz local oscillator signal is generated by a voltage tuned oscillator in the if phase-locked oscillator unit. This oscillator operates in a phase-locked loop which is controlled by a 10-MHz signal from the frequency synthesizer. The 10-MHz signal is applied to if phase-locked oscillator unit Y2 through power monitor CR3 to provide signal level monitoring. The dc voltage, which is developed by the power monitor and is proportional to the 10-MHz signal level, is applied to meter M1 through A6 and switch S1. An if local oscillator tuning output is also produced by the if phase-locked oscillator unit. This dc output, which represents the oscillator frequency control voltage, is applied to out-of-lock detector A5. When the oscillator is out-of-phase-lock, an ac voltage is impressed on the if local oscillator tuning output. This voltage actuates unit A5. The actuation of unit A5 causes IF L.O lamp DS4 to illuminate, provides a relay contact closure for a remote alarm circuit, and creates an amplifier AR1 inhibit condition. The amplifier inhibit signal shuts down 700-MHz amplifier AR1.

f. The 700-MHz if signal (d above) from the if conversion stripline assembly is applied to band reject filter FL1. This filter provides rejection of the 630-MHz local oscillator frequency. Filter FL2, which follows, limits the if bandpass to between 680 and 720 MHz. The output of filter FL2 is applied to amplifier AR1 through directional coupler DC2.

g. Directional coupler DC2 provides an isolated 700-MHz if test input through connector J4; amplifier AR1 provides 45 db of amplification. Amplifier AR1 also provides a de voltage output proportional to the amplified if signal level. This voltage is applied to meter M1 through unit A6 and switch S1. An inhibit signal from unit A5 shuts down amplifier AR1 when phase-lock local oscillator Y1 or Y2 is out-of-phase-lock.

h. The rf mixer receives the 700-MHz signal from amplifier AR1 and mixes this signal with the 7.2- to 7.7-GHz local oscillator signal from rf phase-locked oscillator unit Y1. The resulting 7.9- to 8.4-GHz rf signal is applied to the rf output circuit. The rf mixer also provides a 7.2- to 7.7-GHz rf local oscillator test output to front panel RF LO SAMPLE connector J3. Termination AT4 provides the 50-ohm terminating impedance required by connector J3 when not in use.

i. The rf local oscillator signal is generated by a 1.44- to 1.54-GHz microwave signal source and an X5 frequency multiplier in rf phase-locked oscillator unit Y1. The signal source is phase-locked to the 144- to 154-MHz signal from the frequency synthesizer to provide precise control and stability. An indication of phase lock is provided for monitoring purposes. If the signal source drops out of phase lock, the voltage appearing at this output activates out-of-lock detector unit A5. This action causes RF LO lamp DS3 to illuminate and provides a relay contact closure for a remote alarm. A sample of the frequency control voltage used to maintain the signal source in phase lock is also provided. The frequency control voltage sample is applied to meter M1 through unit A6 and switch S1.

j. The rf local oscillator signal is applied to the rf mixer through power monitor CR4, filter FL5, and circulator HY4. The power monitor provides a dc voltage proportional to the local oscillator level. This voltage is applied to meter M1 through unit A6 and switch S1. Filter FL5 restricts the signal bandwidth to the desired 7.2 -to 7.7-GHz frequency spectrum. Circulator HY4 provides matching between filter FL5 and rf mixer CR2, preventing detuning and rf losses due to mismatch.

k. The 7.9 to 8.4-GHz rf signal (h above) is applied to filters FL3 and FL4 (sheet 11) which are connected in cascade through circulators HY1 and HY2, respectively. Filters FL3 and FL4 ensure that the required 80 db local oscillator isolation is obtained. The circulators are included to prevent filter detuning and provide proper isolation between them. The output of filter FL4 is applied to attenuator AT1 through circulator HY3. Circulator HY3 isolates filter FL4 from signal disturbances and loading effects in the output waveguide run. Attenuator AT1 provides a 0- to 30-db attenuation range to adjust the output power level. From attenuator

AT1, the rf signal is applied to transition CP3 through directional coupler output of transition CP2 is applied to the signal combiner through connector J1. The individually upconverted carriers are combined in the signal combiner (a passive waveguide device HY- 1) for further amplification in the power amplifier subsystem of the AN/TSC- 54.

l. Directional coupler DC3 provides two rf signal samples. One of the samples is applied to the power level monitor unit through attenuator AT2, front panel RF POWER MONITOR connector J7, and RF POWER METER INPUT connector J12. Power level monitor unit A4 operates with RF POWER meter M3, which has preset level controls connected to RF LEVEL lamp DS2 and audible alarm DS5. Lamp DS2 illuminates and audible alarm DS5 is activated when the sampled rf signal level is above or below the preset level. Attenuator AT2 provides the 0- to 3-db attenuation range required for calibration of the power level monitor unit.

2-14. Power Amplification

(fig. FO 2-1, sheet 12)

Signal translation to a transmit frequency is followed by progressive power amplification to a desired carrier level. Amplification can be accomplished by either the HPA or LPA. In both transmitters an initial increase in power is provided by a traveling-wave-tube (TWT) rf amplifier and final amplification is achieved through a klystron electron tube. In the HPA the two-stage amplification produces an 8-kW power level, however, this level is diminished to a 5.25-kW carrier level after losses are incurred by subsequent isolator and passband limiting components.

In the LPA, amplification produces a 1-kW nominal, 1.5kW maximum output power level.

a. In normal operation, the transmit signal from the upconverter is applied to 3 db power splitter 2A3A10 DC1; one port output is connected to the HPA; the secondary part is connected to the LPA through isolator 2A3A10 AT4. The HPA rf input is routed through circulator 2A3A10 AT24, diode switch S6, and 0- to 20db variable attenuator AT1 to the input port of rf amplifier A14. When a fault is detected, diode switch S6 provides a means to protect the TWT by attenuating the rf drive 40 db.

b. Rf amplifier A14 is a traveling-wave-tube amplifier with a self-contained power supply that furnishes the necessary dc operating voltages. The twt device amplifies the transmit signal to a level needed for controllable driving power to the klystron amplifier. Within the twt amplifier, a stream of electrons interacts continuously with the guided electromagnetic wave. The stream and wave move substantially in synchronism and in such a way that there is a net transfer of energy to produce amplification. Rf amplifier A14 provides a minimum power gain of 50 db with a 0.01-mW input signal and is capable of producing an output of 3 watts with the higher-level input signals that prevail during normal transmit operation. The amplifier has an overall response that is flat within 3db over the entire 7.9- to 8.4-MHz transmit range with any 10-MHz segment flat to within 0.3 db. The amplifier attenuates second harmonics at least 15 db below the fundamental frequencies, and suppresses all other spurious signals at least 50 db. The integral power supply derives + 6.6 filament voltage and a -2,200 collector voltage across amplifier pins A and B. Pins D and E are 120-volt common and cathode current monitoring connection points, respectively. Cathode current of the twt is monitored by TEST meter M2, at the transmitter control panel, through operation of test meter selector switch S9.

c. Motor driven attenuator AT6 receives the amplified transmit signal (b above) through a flexible waveguide transition. The XMIT OUTPUT DECREASE INCREASE toggle switch on the transmitter control panel pushbutton switches, on rf power monitor and control panel 1A2A27 (fig. FO 2-4, sheet 1) remove or insert attenuation and, therefore, control the power output of the transmitter by varying the driving power to the klystron amplifier. Motor driven attenuator AT6 provides a 30-db range for this control. Attenuation is varied by an integral 400-Hz, three-phase motor.

(1) The position of CONTROL keylock switch S2 determines which of the two switches will effect the attenuation changes. In the LOCAL position, keylock switch S2 applies + 28 vdc unregulated power to DECREASE switch A2 and INCREASE switch S3. In the PEDESTAL position, + 28 vdc power is applied through filter FL6A4 to energize pedestal control relay K9. When energized, relay K9 applies + 28 vdc unregulated power through contact B1 and B2 to contact 2 of XMIT OUTPUT toggle switch S2. Additionally, low liquid interlock relay K17 contacts B2 and B1 must be closed to obtain the + 28 vdc unregulated power from its source.

(2) In the INCREASE position, the selected output switch connects + 28 vdc unregulated power through filter FL11C1 to energize motor raise relay K22. XMIT OUTPUT toggle switch S2 applies +28 vdc power through contact 1 to energize motor raise relay K22. Thus energized, motor raise relay K22 operates to apply 400-Hz, phase A and B power to motor driven attenuator AT6 in a phase relationship that causes a drive motor rotation that decreases attenuation.

(3) In the DECREASE position, the selected output switch applies +28-vdc unregulated power to energize motor lower relay K23 in an identical manner as that described in (2) above. The attenuator drive motor has a brake that maintains the shaft position when the motor is not running. Two interlocks (limit

switches) interrupt power to the drive motor to prevent damage when the attenuator reaches maximum or minimum attenuation.

d. Directional coupler DC4 provides two 10-db cross-coupled test ports. One port has a waveguide termination, while the other port has a waveguide-to coaxial adapter with a coaxial termination. The latter port is the test translator test point which is used during loop testing and equipment alignment. A waveguide elbow applies the transmit signal to reflection isolator AT19. Reflection isolator AT19 absorbs the reflected power and allows passage of forward power. A direct waveguide-flange connection applies the isolator's output signal to variable attenuator AT10 (e below).

e. Variable attenuator AT10 meters the maximum amount of drive power that can be ultimately applied to klystron and electromagnet assembly A19. The drive power is coupled by input and output direct waveguide-flange connections. Variable attenuator AT10 is set during equipment alignment to limit klystron power at the saturation point. With variable attenuator AT10 preset, motor driven attenuator AT6 can be safely operated over its entire range without overdriving the klystron and electromagnet.

f. Directional coupler DC2 provides two 20-db cross-coupled test ports, one for maintenance test purposes and one for selective monitoring of the klystron drive level. Variable attenuator AT12, attached to one of the test ports, provides a means for calibrating the klystron drive power scale of remote and local rf power meters (para 2-17a). A flexible waveguide transition routes the transmit signal between directional coupler DC2 and klystron and electromagnet assembly A19.

g. The klystron and electromagnet assembly consists essentially of a klystron electron tube and two electromagnets which provide 8 kilowatts of saturated power with an input of 250 mW maximum driving power. The klystron electron tube is operated class C. Although 8 kilowatts of power is developed at the klystron's output port, only a portion of that power remains available after processing; approximately 5.25 kilowatts is applied to the antenna for radiation into space. A flexguide coupler routes the klystron's output to passband limiting microwave components. Both waveguide flanges of the flexguide coupler are jacketed for liquid coolant dissipation of heat.

(1) The klystron electron tube has five cavities and associated tuning elements. Incremental detuning of the elements, in high and low frequency ranges, achieves an overall flat bandpass response with optimum power conversion. When turned to encompass the five transmit channels, the klystron tube, in either half of the 7.90 to 8.4-GHz transmit band, exhibits a 35-percent efficiency. Modified power supply PS2 (fig. FO 2-8, sheet 7) supplies the necessary - 13 kvdc and - 13.0075 kvdc operating power for the klystron electron tube.

(2) Magnet power supply A21 supplies + 150-vdc power across the series-connected upper and lower electromagnets of klystron and electromagnet assembly A19. The two electromagnets are series connected and are liquid cooled for heat dissipation.

2-15. Transmission Passband Limitation

(fig. FO 2-1)

The amplified transmit signal is conditioned through various passband limiting components before being applied to the antenna. This conditioning emphasizes the elected transmit channel frequency by allowing its relatively unimpeded passage while attenuating harmonics and suppressing adjacent frequencies. The passband limiting components provide a flat frequency response that encompasses the five transmit channel frequencies. Three power sampling directional couplers are included in the microwave path to the antenna components. Three 50-db directional couplers individually extract forward and reflected power samplings which are used for illuminating fault lamps or visual observation on meters. Detailed discussion f fault detection is covered in paragraphs 2-18 through 2-32 and the rf metering circuits are discussed in paragraph 2-17.

a. The klystron output signal is applied through directional coupler DC3 (sheet 13) and y-shaped adapter AT8 to reflection isolator AT14. Adapter AT8 also provides a 0.187-inch diameter view passage for arc detector amplifier A13 (b below). Physical length of his view passage is such that it falls below the cutoff frequency and no loss is incurred. Waveguide adapter LT8 is liquid cooled and it interconnects its three adjacent devices by means of direct waveguide-flange mating.

b. Arc detector amplifier A13 consists of a photosensitive semiconductor element, a detector circuit, and a test lamp. In normal transmitting operations, he device detects arcs by literally looking directly into he output port of klystron and electromagnet assembly A19, (sheet 12). The detector is physically oriented on waveguide adapter AT8 (sheet 13) so that its photosensitive element is exposed to the klystron's output port by direct alignment through the adapter's drilled view passage. Any luminous arcing that occurs within the klystron electron tube triggers an arc detector circuit (para 2-31). The test lamp of the detector can be illuminated to simulate an arc for fault circuit test purposes; the lamp illuminates a drilled chamber and a milled passage which directs part of the light to the photosensitive element and triggers the detector circuit.

c. Rf reflection isolator AT14 absorbs reflected power within the microwave path to the antenna by means of its integral air and liquid-cooled dummy ads. The device provides at least 20 db isolation with

a 0.3-db, or lower, insertion loss across the transmit band. The signal is applied to directional coupler DC5 by a direct waveguide-flange connection.

d. Harmonic filter FL7 attenuates all harmonics the selected transmit channel frequency. Specifically, it attenuates the second and third harmonics, 45 and 30 db, respectively, and attenuates all other harmonics 20 db. Longitudinal cooling fins on the filter dissipate heat by radiation and convection. Two waveguide elbows and straight waveguide transition CP9 routes the transmit signal to bandpass filter FL8 (e below).
The waveguide transition effects a change to a larger rectangular waveguide cross section.

e. Seven fixed-tuned cavities within bandpass filter FL8 provide a response that rejects transmitter noise from occurring in the receive frequencies band. Since the receiver and the transmitter share a common antenna, unsuppressed transmitter noises could detrimentally affect the receive signal noise figure. Bandpass filter FL8 attenuates the noise at least 25 db and also functions as a bandpass filter for the transmit frequencies. After initial factory tuning, the filter's tuning elements are permanently sealed and locked with adhesive compound, and the filter is encased within a cylindrical jacket. Liquid coolant circulated through this jacket extracts heat from the bandpass filter.

f. Directional coupler 2A3 DC6 (sheet 14) applies the filtered transmit signal (d and e above) to waveguide switch 2A3 S3 by direct waveguide-flange connections. The waveguide switch has two positions. In one position, the switch directs the HPA transmit signal to mode launcher All (para 2-16a) and connects the LPA rf transmission line to dummy load 2A3 AT17. In the other position, the switch connects the HPA to electrical dummy load 2A3 AT17 (h below) and the LPA to mode launcher All. The dummy load permits testing of the HPA transmitting function without radiating a signal at the antenna.

g. Waveguide switch 2A3A10S3 is controlled by the LPA (fig. FO 2-4, sheet 2). The switch is shown in position 1. When set to position 2, the contactors move so that E-D, G-H open and K-L, P-N close. In addition, the A input to the motor is connected and the B input opens. In position 1, waveguide ports 1-2 and 3-4 are connected; in position 2, ports 1-4 and 2-3 are connected. Switches at LPA 2All activate the LPA or HPA SELECT inputs (P22 pin A or B). Waveguide switch contacts (pins P-N and E-D) are used for LPA operational status and command inhibit signals. The G-H and L-K contacts are used for transmitter control panel 2A3A7 status and relay control.

2-16. Signal Transmission

(fig. FO 2-1, sheet 14)

The amplified and conditioned transmit signal (para 2-14 and 2-15) is applied through functional microwave components to four waveguide feed assemblies which radiate the rf energy. The microwave components smoothly effect transverse field mode transitions to pass the rf energy to differently-configured waveguides and movable joints. Power dividers progressively subdivide the rf energy into equal amounts for application to the four waveguide feed assemblies. Finally, four specially-shaped DIELGUIDEs direct most of the radiated energy to four parabolic reflectors that are adjoined in a cloverleaf array.

a. Mode launcher All (para 2-15f) receives the rf energy from waveguide switch S3. Energy transfer is by means of a direct waveguide-flange connection and in a rectangular TE 1,0 (transverse electric) propagation mode. The mode launcher's progressively-varying cross sectional configuration effects a mode change to circular TE 0,1 mode. From a rectangular input port, the launcher body diverges to a cross shape in which a TE 2,0 mode prevails. Beyond this point, the center area of the cross shape blooms to a circular output port, completing the change to TE 0,1 mode. The mode launcher is convection cooled.

b. Rotary joint assembly A15 is a simple gap in the waveguide. Dual annular bearing assemblies maintain the gap clearance and alignment during antenna changes in azimuth. A preformed packing seal prevents the loss of waveguide pressurization and an absorber ring attenuates any undesired mode energy that enters the joint gap. To energy in the TE 0,1 mode, the rotary joint appears as a straight section of circular waveguide.

c. Two self-aligning waveguide flanges comprise fold joint assembly A10. The lower half of fold joint is secured directly to the rotary joint (b above). The upper half of the fold joint, secured within the mast assembly, mates with the lower half when the mast is fully raised. Thus mated, the joint effectively forms a continuous waveguide section for the unimpeded transfer of energy to mode filter FL1 (d below). A bellows type, rubber-impregnated canvas boot installed on the fold joint prevents loss of waveguide pressurization at the surface-mated joint halves. The boot also excludes dust and moisture from the waveguide when the mast is folded.

d. Mode filter FL1 passes rf energy with minimum loss and also removes resonances that may be incurred by undesired modes. In the transmit frequency range, the dominant TE 0,1 modes is the only propagating mode in the waveguide that does not have longitudinal wall currents; therefore, small gaps at waveguide joints or grooves machined in waveguide walls do not affect desired transverse electric fields. Undesired modes (12 of which can exist in the waveguide) are affected and suppressed. Plastic compound, energy-absorbing rings, are recessed in 10 grooves within the mode filter to trap and absorb the small amounts of rf energy developed by the undesired modes. Attenuation or absorption of these stray energy waves

preclude resonances within the waveguide. Mode filter FL1 applies the rf energy straight through a 43-inch long section of circulator waveguide assembly (2A4W4) to the input port of launcher divider A8 (e below)

e. Launcher divider A8 restores rf energy propagation to a rectangular mode in a manner almost reversed from that which occurs within mode launcher All (a above). In the launcher divider, the housing cross section converges from a circular to a rectangular output port that is twice as long as a normal waveguide port. The converging shape provides for TE 1,0 mode, uniformly distributed energy transfer to power divider All (f below).

f. Two opposing waveguide elbows, having their input ports oriented in tandem at a common flange comprise power divider All. The power divider splits its input rf energy and diverts the two portions through separate waveguide sections to left- and right-hand halves of the reflector assembly.

g. The transmit rf energy is applied in equal amounts to rotary step coupler assemblies A50 and A51. Each rotary coupler has several uniquely linked disks with rectangular apertures. Rotating incrementally as the elevation angle varies, the rectangular apertures impart a twist configuration for rf energy transfer to a power divider. The rotary coupler is capable of handling twist angle variations of + 55 percent from neutral (straight-through setting). At the maximum angle variation, a 550 twist is achieved over the 3-inch length of the coupler. Direct waveguide-flange connections apply the rf energy to the associated power divider. The power dividers are waveguide T's that provide a second subdivision of rf energy. With one exception, individual waveguide sections routed equal amounts of rf energy directly to waveguide feed assemblies. The exception prevails at one output port of power divider A51All. This output branch has an additional function in that it provides rf power samplings (h below).

h. Directional coupler W7 is a 34-inch long formed section of waveguide with a short coupling section mounted across it. Two drilled apertures between the sections provide - 54 db signal coupling to the sample output ports. One port has a waveguide-to-coaxial adapter with a coaxial termination. The other sample port of the directional coupler provides a transmit signal sample used by the test translator. The coupler passes the bulk of the rf energy to the waveguide feed assembly (i below).

i. Each of the four waveguide feed assemblies has, in transmit signal processing order, a crossmode transducer (duplexer), a 90 percent differential phase shifter (polarizer), and a multichoke horn mounted within a feed support housing. The duplexer provides bi-directional coupling to facilitate concurrent transmit and receive operations. The polarizer is a section of iris-loaded circular waveguide. It produces a 900 differential phase shift between the polarization alignment with the irises and the orthogonal input polarization. With the irises set at 45° clockwise angle with respect , the linear input polarization, the output energy is circularly polarized in a right-hand direction. The circularly polarized energy is applied directly to the multichoke horn. The horn is designed and physically oriented to provide nearly equal E- and H-plane beam-widths and phase centers. The horn, duplexer, and polarizer respond with equal effectiveness at receive and transmit frequencies ranging from 7.25 GHz to 8.4 Hz. During transmission, each waveguide feed assembly beams rf energy forward into its associated DIELGUIDE assembly (' below).

j. A DIELGUIDE assembly essentially consists of a support can, dielectric guiding structure, a subreflector, and a cone-shaped radome jacket. The dielectric guiding structure redirects the rf energy that would normally be lost in the antenna side lobes. The electric material of the guiding structure is oriented an angle that causes deflection of the transmit output energy that encounters it. Thus, the bulk of the transmitted energy beamed directly at the subreflector plus the peripheral energy deflected to the subrelector is utilized, to provide a 75 to 80 percent efficiency. Two flatted areas on the dielectric guiding structure effectively tailor the feed patterns to conform with the asymmetrical main reflector contour to preclude or minimize energy spillover to adjacent reflectors. The subreflector turns the beamed and detected rf energy onto the main reflector which provides final beam shaping for energy radiation to the selected satellite. The support can and radome jacket hold the dielectric guiding structure and subreflector correct orientation at the main reflector's focus point, eliminating a requirement for support struts. The transmitted signal, progressively boosted in frequency, amplifier, shaped, and subdivided into four equal portions, is then radiated into space in four parallel beams.

2-17. Rf Metering Circuits

(fig. FO 2-1)

a. Directional coupler 2A3A1ODC2 (sheet 12) probes a 20-db down sampling of the driving power aped to klystron and electromagnet assembly A19. The drive power sampling is applied by direct waveguide-flange connections, through variable attenuator 712, to waveguide-to-coaxial adapter CP2. The sampling is then applied through a cable, an rf power ad, and a power meter amplifier to a display meter the transmitter control panel 2A3A7 (sheet 14).

(1) Variable attenuator AT12 (sheet 12) provides means for adjusting the drive sampling level to

achieve correlated meter indications. Cable W7 routes the attenuated sampling to input jack J1 on transmission line rf switch S1.

(2) Control voltages are applied by either 1A2A27 or 2A3A7 METER SELECT switch S1 (fig. FO 2-4, sheet 1) to the transmission line rf switch driving motor. The position of CONTROL keylock switch S2 determines which METER SELECT switch has control of the transmission line rf switch.

(*a*) In the LOCAL position, the keylock switch connects +28 vdc unregulated power to wiper contact C1 of METER SELECT switch S1 (1A2A27).

(*b*) In the PEDESTAL position, the keylock switch applies +28 vdc unregulated power to the coils of pedestal control relays K9, K10, and K11. With relay K9 energized, +28 vdc is applied to wiper contact C1 of meter select switch S1 (1A2A27).

(*c*) When the active selector switch is set to DRIVE, the driving motor of switch S1 rotates until switch position No. 1 is reached. At this point, a notch in an integral motor-control wiper disk falls opposite the position No. 1 control voltage contact, and the driving motor operating voltage circuit is opened.

b. Concurrently, the mechanically linked wiper contact of rf transmission line switch S1 (sheet 14) is positioned to pass the klystron drive power sampling from input jack J1 to switch output jack J6. Cable W8 connects the selected rf sampling to rf head A16. Within the rf head, if-power-produced heat varies the resistance of a thermistor in a voltage divider network. The resistance change causes a corresponding voltage change at the input (J2) to rf amplifier A15. Rf amplifier A15 senses the voltage change, with respect to an rf reference input, and produces identical driving currents to its output pins J1-J and J1-K, with pins J1-M and J1-L used as the respective return pins. The J1-J output is connected through the rf power meter, at the antenna pedestal, and returned through pin J1-M. The J1-K output of rf amplifier A15 is connected through the rf power monitor and control panel rf power meter in the shelter and returned through pin J1-L (fig. FO 2-4, sheet 1).

c. Directional coupler DC6 provides 50-db down power samplings of transmitter reverse power. Directional couplers DC6 and DC7 (10-db) together provide samplings of transmitter forward power (sheet 14). Variable attenuators AT18 and AT21 provide adjustment of forward power samplings, and variable attenuator AT16 provides adjustment of reverse power samplings, to achieve accurately correlated meter indications. Waveguide-to-coaxial adapters CP10 and CP3 pass the attenuated forward and reverse power samplings through cables W5 and W6, respectively, to transmission line rf switch S1. Waveguide-to coaxial adapter CP4 passes the attenuated forward power sampling through cable W13 to transmission line rf switch 2A3S2.

d. Coax switch 2A3S2 (fig. FO 2-1, sheet 14 and 2-4, sheet 6) is operated from the LPA and permits selection of either the HPA or LPA for power monitoring by on-line transmitter output power assembly 1A2A27A4. When the LPA is switched to on-line operation a +28 vdc input is routed through HPA OFF LINE switch 1A2A27A4S2 to rf transmission line switch 2A3S2. This input connects the No. 2 port to the IN port, permitting the LPA rf output to be monitored. This rf level is routed through 40-db directional coupler DC100, variable attenuator 2A3AT100, waveguide-to-coaxial adapter 2A3CP100 to switch 2A3S2.

e. The output is routed over cable W18 to rf switch 2A3A10S5. This switch (fig. FO 2-4, sheet 6) normally connects the input from switch 2A3S2 to switch 2A3A10S2. When on-line transmitter output power assembly 1A2A27A4 METER ZERO switch S2 is pressed, +28 vdc causes rf transmission line switch 2A3A10S5 to connect attenuator AT22 into the line through connectors J2 and J3 as a known reference for meter zeroing. When the METER ZERO switch is not pressed, the rf level is routed through J1 and J3 connectors through cable W16 to rf transmission line switch 2A3A10S2. This switch (fig. FO 2-4, sheet 7.1) is controlled by on-line transmitter output power assembly RANGE switch 1A2A27A4S1. When set to the up position, the low range is selected, and when set to the down position the high range is selected. The + 28 vdc power to operate switch 2A3A10S2 is routed through switch 1A2A27A4S1, over cables W15 and W16 to the rf transmission line switch (fig. FO 2-1, sheet 14). The up position causes attenuator 2A3A10AT3 to be bypassed; the down position connects the attenuator in series with the line through cable W17. The attenuator permits level setting of the rf input.

NOTE

A discrepancy in readings may be observed when switching from the upper to lower scale or vice versa. This is caused by the accuracy tolerances of auto range power meter amplifier 2A3A10A18 and losses of attenuator 2A3A100AT3 and cable 2A3A10W17 of the range selection circuit. Initial calibration should be performed on the scale used most often. When changing scales, meter must be recalibrated.

f. From switch 2A3A10S2, rf power is connected to rf power head 2A3A10A22 through isolator 2A3A10CP14 which is a dc block to prevent ground loops. The rf head absorbs rf power and provides a dc level to 40 db auto range meter amplifier 2A3A10A18.

g. The 40-db auto range meter amplifier (fig. FO 2-1, sheet 14) measures the average power absorbed by rf power head 2A3A10A22. The amplifier provides automatic ranging of four scales; the outputs are sent to on-line

transmitter output power assembly range indicators (fig. FO 2-4, sheet 7.1). The four outputs (P79, pins F, G, H, J) are routed over cables W15 and W16, through contacts of relay 1A2A27A4K4 to the range indicators. Relay operation is controlled by both the LPA and HPA; it is energized from the LPA, but can be deenergized by setting HPA OFF LINE switch 1A2A27A4S2 to the down (METER ZERO) position. The amplifier output is sent to the power meter.

h. The rf input is displayed on power meter 1A2A27A4M1 and is also monitored by the meter/relay assembly. If the rf level falls below or rises above the present limits, a relay energizes, connecting + 28 vdc power from terminal board TB2-2 (fig. FO 2-4, sheet 6) through the relay contacts (sheet 8) to buzzer DS1.

i. Meter zeroing control for 40 db auto range power meter amplifier is provided by METER ZERO potentiometer 1A2A27A4R1. Cables W15 and W16 connect the potentiometer to amplifier connector P79 pins K, L and M.

j. For monitoring forward power from the transmitter control panel, or the rf power monitor and control panel, the active meter select switch (fig. FO 2-4, sheet 1) is set to FWD and the coaxial section of switch S1 rotates to a stop position No. 2, thus connecting the forward power sampling between jacks J2 and J6. Setting the active meter select switch to REV similarly causes switch S1 to connect the reverse power sampling between jacks J3 and J6. The selected power sampling at output jack J6 is subsequently processed and routed to rf power meters as described above. For monitoring transmitter forward power at the on-line transmitter output power assembly power meter 1A2A27A4M1 coaxial switches 2A3S2, 2A3A10S5 and 2A3A10S2 are operated as described above (fig. FO 2-4, sheets 6 and 7.1).

k. Identical rf power meter zeroing potentiometers are provided for either the shelter (rf power monitor and control panel) or antenna pedestal zero-set calibration of the power meter circuit. Each potentiometer is adjusted so that the associated rf power meter indicates zero when no rf power sampling is applied. The position of CONTROL keylock switch S2 (fig. FO 2-4, sheet 1) determines which meter circuit is active. When set to LOCAL, the keylock switch removes energizing voltage from a pedestal control relay (c (2) above), placing the METER ZERO control of the rf power monitor and control panel into the power meter circuit. When set to PEDESTAL position, the keylock switch connects an energizing voltage to the pedestal control relay, placing the transmitter control panel RF METER ZERO control into the power meter circuit. The on-line transmitter output power assembly rf power meter 1A2A27A4 circuit is active regardless of the setting of the CONTROL keylock switch and will indicate transmitter forward power as long as the transmitter output is present. Placing the ALARM toggle switch to the INACTIVE position places the ZERO SET control in the power meter circuit.

l. Klystron beam, body, and magnet currents can be selectively applied across TEST meter M1 on the transmitter control panel (fig. FO 2-4, sheet 4) for monitoring purposes. Three pairs of contacts on switch S8 are used to connect the meter in parallel with current shunts to automatically provide correct meter ranges.

(1) In the KLYSTRON BEAM CUR. position, the negative side of meter M1 is connected to terminal 3 (negative) of meter shunt resistor R4. The position side of meter M1 is connected to terminal 4 (positive) of meter shunt resistor R4. With this current path completed, TEST meter M1 deflects to indicate klystron beam current.

(2) In the KLYSTRON BODY CUR. position, the negative side of TEST meter M1 is connected to terminal 1 (negative) of meter shunt resister R2. The positive side of meter M1 is connected to terminal 2 (positive) of meter shunt resistor R2. With this current path completed, TEST meter M1 deflects to indicate klystron body current.

(3) In the MAGNET CUR position, the negative ;side of TEST meter M1 is connected to the negative side of meter shunt resistor R3. The positive side of meter shunt resistor R3 is connected to the positive side of TEST meter M1 to indicate klystron magnet current.

m. Switch S9 connects TEST meter M2 for monitoring the klystron beam voltage. In the KLYSTRON BEAM VOLTS position, the negative side of meter M2 is connected to beam volts monitor terminal PS1-B. The positive side of meter M2 is connected to beam supply return terminal PS1-A. With the current path thus completed, TEST meter M2 deflects to indicate he klystron beam voltage.

2-18. General Analysis of Fault Detection and Indication Circuits

The fault detection and indication circuits incorporated in the AN/TSC-54 detect marginal operating conditions and equipment malfunctions. Upon detecting undesired conditions, the circuits provide either visual indications, initiate audible alarms, or inhibit drive and high voltage power.

a. Trip points of some detection circuits illuminate white or amber indicators that immediately alert the equipment operator that a marginal condition warrants minor readjustment. Circuits that monitor more significant operational parameters illuminate red indicators and, in many cases, also initiate audible alarms when safe operating conditions are exceeded. Other detection circuits disclose the more serious conditions and automatically inhibit low-level signals from which dystron drive power is derived and remove the klystron beam voltage to preclude serious equipment damage.

b. When indications of the lesser faults are noted, limited operation under close observation of the system can be continued but only when fully justified by operational urgency. Fault reset provisions allow removal of the audible alarm and illuminated fault indications that latch in the on condition upon initiation. Fault lamp test circuits provide for combined testing of all fault lamp driving circuits.

2-19. Low Rf Power Detection
(fig. FO 2-4)

a. The low rf power indication is based on the level of signal available at the forward power sample port of directional coupler DC3 (fig. FO 2-1, sheet 13). The forward power sample is applied through variable attenuator AT2, waveguide-to-coaxial adapter CP7, and low-pass filter FL6 to rf detector A8. The variable attenuator is adjusted to establish a klystron vswr trip point. Low-pass filter FL6 passes transmit band frequencies but rejects their harmonics by attenuating them 50 db. Rf detector A8 removes the negative portions from the sample signal and passes a varying-level positive dc signal through coaxial cable W12 to detector amplifier A12 (sheet 4). Within detector amplifier A12, the forward power signal is developed across a resistor network composed of resistors R1, R2, and R6, and coupled by resistor R4 to pin 3 of the dc amplifier. Reference voltage levels of approximately-7 vdc at pin 10 and 6 vdc at pin 2 are established by a voltage divider consisting of resistors R3 and R5, diodes CR3 and CR1, and a 1-kilohm resistor within isolator power comparator A8 (sheet 5). Small voltage drops across the junctions of diodes CR1 and CR3 account for the less negative reference level at pin 2 of the dc amplifier. The two diodes also prevent the output at pin 10 from affecting the reference input at pin 2.

b. The dc amplifier compares its forward power sample and reference inputs, and superimposes the difference onto the output reference level at pin 10. This forward power detect signal is applied through connector pins P46-F and J2-M (sheet 5) to input pin C6-5 of low rf sensing circuit A6. A level-set potentiometer within the sensing circuit is preset to trip the circuit when the transmit output power drops below the minimum acceptable level. At that marginal point, a level detector in the sensing circuit forward biases a transistor into saturation, thus completing a return path for indicator lamp driving current. With the current path completed, +28 vdc is applied cross transmitter control panel LOW RF POWER indicator lamp DS11 (white) and returned through the saturated transistor to the +28-vdc common terminal. Concurrently, upon application of a +15-vdc fault signal to latching circuit No. 2, a +28-vdc output is provided through connector pin J2-Q and RF1 filter FL7B4 (sheet 6) which energizes relay K3 in the rf power monitor and control panel. With relay K3 energized +28 vdc is provided to illuminate XMIT FAULT indicator lamp A1 and sound audible alarm DS11 located on the front panel of rf power monitor and control panel 1A2A27. The fault indicator is one side of a split-lens indicator switch which when pressed, following a fault indication, silences the audible alarm and illuminates the other side of the split-lens indicator (fig. FO 2-4, sheet 6).

c. Low rf power is also detected by the circuitry in on-line transmitter output power assembly meter assembly 1A2A27A4M1. The low power point is operator set by the lower fault limit adjustment on the assembly front panel. The transmitter forward power sample is applied to the rf power meter through rf switches and power head J4 as described in paragraph 2-17. When the rf power drops below the established lower limit, alarm 1A2A27A4DS1 sounds (para 2-17*n*). The power meter also provides a visual indication of the amount by which the rf power has fallen below the lower fault limit (fig. FO 2-4, sheet 6).

d. It is possible for transients to generate a false LPA on-line command and initiate a series of events that will switch the LPA on-line, operate the LPA waveguide switch, convert 28 vdc through contacts of this waveguide switch that energizes switch 2A3S2 to the LPA power monitor position, and shut down the LPA (if the HPA is on-line). This type of condition may occur during performance of preventive or corrective maintenance routines at the LPA. If the HPA was online and personnel observed that the rf level had dropped (due to the conditions resulting from a transient), it might at first be assumed that the HPA has malfunctioned and is not transmitting. Before assuming that an HPA fault exists, check for HPA power output by momentarily setting HPA OFF LINE switch 1A2A27A4S2 to HPA OFF LINE. (This action opens the 28 vdc path from the LPA waveguide switch to switch 2A3S2, and connects switch 2A3S2 to the HPA rf output line.) If the power meter indicates the same (normal) rf output level as before occurrence of the transient, then there is no HPA malfunction. If there is no indication on the meter then an HPA fault condition does exist.

NOTE

LPA circuits automatically shut off LPA rf output power when both HPA and LPA are on-line at the same time. For this reason the meter will indicate no rf output after the LPA is switched on-line and switch 2A3S2 selects the LPA rf output line.

2-20. Low Waveguide Pressure Detection
(fig. FO 2-4)

Low waveguide pressure switch S4 (sheet 5) directly

controls low waveguide pressure indications. Under normal waveguide pressurization of 1 psig nominal air pressure, switch S4 remains open. When the pressure drops below the minimum acceptable level, air pressure switch S4 closes and applies +28 vdc unregulated power through connector pins J1-F and P26-FF to two separate indicators.

a. Application through diode CR16, illuminates WG PRESSURE indicator lamp DS9 (amber) located on the transmitter control panel 2A3A7. Diode CR16 prevents interaction between the operational and lamp test segments of the low waveguide pressure circuit.

b. Applied through pin a of connector J2 and RF1 filter FL13-C-1, located in the primary power distribution panel 1A15, the +28 vdc illuminates LOW WG PRESS indicator lamp DS2 (amber) located on the rf power monitor and control panel 1A2A27 (sheet 6).

2-21. Low Liquid Warning Detection
(fig. FO 2-4)

Low liquid warning switch S2 in heat transfer assembly A2 (sheet 3) directly controls the low liquid warning indications. The switch normally remains open under a satisfactory liquid coolant level condition; however, it closes when the coolant level drops below the minimum acceptable level. When closed, low liquid warning switch S1 applies +28 vdc unregulated power through pins J2-C and J2-B, filter FL1A1, and pin z of connector W1P26 (sheet 5) to LOW LIQUID WARNING indicator lamp DS1 (amber) on the transmitter control panel. Since pin 2 of the indicator lamp connects directly to ground, indicator DS1 illuminates and remains illuminated until equipment power is shut down or the coolant is replenished.

2-22. Low Particle Filter Coolant Flow Detection
(fig. FO 2-4)

Particle filter coolant flow switch S3 in the outboard full flow filter and purity loop (sheet 3) is located in the coolant flow line between the three micron full flow filter and the heat exchanger 2A3A3. The switch remains open as long as a satisfactory flow of coolant is maintained through the three micron filter. Any abnormal decrease in coolant flow rate, due to clogging of the particle filter or any other faulty condition, causes the switch to close. Upon closing the switch applies +28 vdc unregulated power through filter FL1C1 and pin P26-NN (sheet 5) to illuminate LOW PARTICLE FIL COOL FLOW indicator lamp DS2 (amber) on the transmitter control panel. Indicator DS2 remains illuminated until equipment power is shut down.

NOTE

This indicated fault is normally corrected by replacement of the three micron filter.

2-23. Low Coolant Temperature Detection
(fig. FO 2-4)

Low coolant temperature switch S2 (sheet 3) directly controls two low coolant temperature indicators and indirectly controls a liquid heater. The indicators and heater are operated simultaneously. Switch S2 remains closed until the minimum acceptable coolant temperature is achieved, then opens and remains open while the temperature is at or above the minimum point. When closed, the switch applies +28 vdc unregulated power to energize liquid heater relay K1 and through diode CR5 to illuminate LOW COOL TEMP indicator lamp DS4 (amber) on the transmitter control panel (sheet 5) and LOW COOL TEMP
indicator lamp DS7 (amber) on rf power monitor and control panel A27 (sheet 6). Both indicators illuminate and remain illuminated until the coolant temperature rises above the minimum level. Operation of liquid heater relay K1 controls the application of power to heater HR1. Heater power is removed when the coolant becomes heated to a satisfactory temperature and the +28 vdc is removed from the coil of liquid heater relay K1.

2-24. Waveguide Flow and Collector Flow Detection
(fig. FO 2-4)

Liquid flow rate switches S4 and S5 (sheet 3) are connected in series to the +28 vdc regulated power source. Either switch (but not both) can simultaneously illuminate an associated fault indicator and energize flow switches relay K19. Flow switches S4 and S5 are shown in their fault-detect positions. Under normal coolant flow conditions, flow switch S4 applies +28 vdc regulated power through switch S5 to energize flow switches relay K19. When either coolant flow rate drops, the respective switch operates to initiate a fault indication. If the waveguide and dummy load flow decreases, switch S4 operates to remove +28 vdc power from the collector flow switch, and the collector flow indicator function is inhibited. If the collector flow rate decreases, flow switch S5 resets to its fault-detect position by removing the +28 vdc power from flow switches relay K19 and applying the +28 vdc to pin E2-9 of latch circuit No. 1 and to the gate of a silicon controlled rectifier (SCR) circuit (sheet 6). The SCR applies +28 vdc (through reset circuits) to illuminate COLLECTOR FLOW indicator lamp DS25 (red). The indicator remains illuminated until a momentary interruption of the +28 vdc power, by means of fault reset switches, resets latch circuit No. 1.

2-25. Filament Cooling Detection
(fig. FO 2-4)

Blower motor interlock switch S5 (sheet 2) controls the filament cooling indication. Assuming normal operation

and a normal supply of liquid coolant, +28 vdc unregulated power is applied through contacts B2 or B1 of low liquid interlock relay K17 (sheet 1) and blower motor interlock switch S5 (sheet 2), to energize blower motor interlock relay K14 and 60 second hold relay K8. Relay K14 operates and applies +28 vdc to energize filament power relay K13 which controls the application of filament power. Conversely, when the cooling airflow rate drops abnormally, blower motor interlock switch S5 opens and blower motor relay K14 deenergizes. Under this fault condition, FILAMENT COOLING indicator lamp DS24 (red) illuminates and remains in that state until equipment power is shut down or satisfactory filament cooling airflow is restored.

NOTE

This fault circuit is not included in the fault reset circuit.

2-26. Antenna Sector Limit Detection
(fig. FO 2-4)

Transmit sector switch S2 (sheet 1) directly controls antenna sector limit indications; however, only during normal transmit operation. Dummy load bypass relay K3 disconnects the fault detect circuit whenever transmit power is being diverted into the dummy load. For antenna elevation positions of +7.5° or greater, transmit sector switch S2 remains closed and continuously applies +28 vdc unregulated power, through the azimuth drive assembly and dummy load bypass relay K3, to sector limit relay K2. While the antenna remains positioned above the minimum elevation angle, relay K2 remains energized and its associated fault indicator remains extinguished. However, transmit sector switch S2 is mechanically opened each time the antenna elevation angle is decreased below +7.5°. Opening of the switch breaks the +28 vdc power path, sector limit relay K2 (sheet 3) deenergizes, and the +28 vdc regulated power is applied to input pin E1-4 of latch circuit No. 1 (sheet 6). Within the latch circuit module, the applied +28 vdc fires a SCR which completes a current path between pins E2-10 and E5-10. In the latched state, +28 vdc power is applied from pin E5-10 to illuminate ANTENNA SECTOR LIMIT indicator lamp DS26 (red). Indicator DS26 remains illuminated until the antenna is again raised above +7.5° and the fault circuit is reset. The sector limit circuits also output a signal to LPA 2A11. The 28 vdc unregulated power through switch S2 to relay K2 is also sent through arc suppression circuit CR1-C1 in relay box assembly 2A3A9 to the LPA elevation interlock circuit.

2-27. Interlock Detection
(fig. FO 2-4)

Interlock relay K5 (sheet 3) controls interlock indicators at the antenna pedestal and in the equipment shelter. Additionally, the relay initiates an audible alarm in the shelter. Under normal operating conditions, +28 vdc unregulated power is applied through the interlocks and contacts of dummy load bypass relay K3 to interlock relay K5. An alternate path for the +28 vdc includes MOUNT SAFE toggle switch S2. When power is applied, interlock relay K5 remains energized and the associated interlock indicator circuit remains in its quiescent (off) state. Immediately upon the inadvertent opening of a mechanical interlock, or the manual positioning of switch S2 to the MOUNT SAFE position, the +28 vdc power path is broken, and interlock relay K5 deenergizes. With interlock relay K5 deenergized, + 28vdc regulated power is applied to input pin E6-2 of latch circuit No. 4. Then applied +28 vdc fires an SCR within the latch circuit module, thus closing a current path for the two interlock indicators. The +28 vdc at pin E9-3 is applied to illuminate INTERLOCK indicator lamp DS19 (red) on the transmitter control panel (sheet 6). The +28 vdc at pin E9-5 is applied to illuminate INTERLOCK indicator lamp DS1 (red) on rf power monitor and control panel 1A2A27. Both indicators remain illuminated until power is shut down or the fault circuit is manually reset. The fault signal applied to pin E6-2 of latch circuit No. 4 also initiates an audible alarm. The MOUNT SAFE switch also provides additional LPA 2A11 interlock contacts for personnel safety. Twenty-eight vdc power from the LPA is routed through the A-B contacts of switch S2, then back to the LPA interlock circuits.

2-28. Body and Magnet Flow, High Coolant Temperature, and Low Liquid Interlock Detection
(fig. FO 2-4)

Four parallel fault detect circuits are separately controlled by liquid flow, liquid temperature, and liquid level actuated sensing switches. The four circuits operate in the same manner, except for method of initial fault sensing.

a. For example, a normal body and magnet coolant flow keeps body and magnet flow switches S3 and S6 (sheet 3) closed, and switch S3 continuously applies + 28 vdc unregulated power to the coil of body and magnet flow relay K18. The relay remains energized and its associated indicator fault circuit remains quiescent since a fault signal (+28 vdc regulated power) is not being applied. When the coolant flow rate drops abnormally, body and magnet flow switches S3 and S4 open and relay K18 deenergizes to apply +28 vdc to input pin D6-4 of latch circuit No. 4. The applied +28 vdc fires an SCR within the latch circuit module and applies + 28 vdc regulated power (through a remote reset circuit) from pin D7-8 and pin D9-1 to illuminate BODY & MAG FLOW indicator lamp DS-22 (red). Indicator DS-22 remains illuminated until the fault circuit is manually reset.

Concurrent with indicator illumination, a remote alarm initiate signal is also generated at pin D10-9 of latch circuit No. 4 (sheet 6).

b. High coolant temperature switch S1 (sheet 3) opens when it senses an abnormally high coolant temperature condition. Circuit operation following the initial fault detection is in the same manner as that described in a above, except as follows: System coolant high temperature relay K21 deenergizes and its closed contacts apply a firing current to an SCR in latch circuit No. 4 (sheet 6). The latch circuit module applies power to illuminate HIGH COOL TEMP indicator lamp DS21 (red).

c. Low liquid interlock switch S2 (sheet 3) in heat transfer assembly A2 opens when it senses an abnormally low coolant level. Following this initial fault-detect action, the circuit operates in the same manner as the circuit described in a above, with the following exceptions: low liquid interlock relay K17 deenergizes, and its closed contacts A2 and A3 apply a firing current to an SCR in latch circuit No. 4 (sheet 6), which, in turn, applies power to illuminate LOW LIQUID indicator lamp DS20 (red).

2-29. Klystron and Electromagnet Low and High Currents Detection

(fig. FO 2-4)

Three fault circuits within the AN/TSC-54 detect abnormal currents associated with klystron operation. The circuits differ in their fault sensing and reference level inputs; however, once detected by identical level detectors, the fault signals follow parallel processing paths and produce similar results. Whether the fault is low magnet current, a high body current, or a high beam current, it triggers an associated latch circuit. This action illuminates a fault indicator lamp, initiates the audible alarm, and activates protective circuits that immediately disable the high voltage and high power functions of the equipment. The latch circuit maintains the fault indication, audible alarm, and protective inhibits until equipment power is shutdown or the fault circuits are manually reset. The high and low current conditions are indicated by separate illuminated indicators on the transmitter control panel and by a common FAULT indicator in the equipment shelter.

a. A low magnet current condition is sensed by level detector A1 (sheet 4). A voltage level developed by the magnet current flow at the junction of shunt resistor R3 and resistor R2 is applied to level detector A1. The level detector compares the signal voltage level with a +15 vdc reference level derived at the junction of resistors R2 and R3. Resistor R4 couples the reference voltage to pin 3 of the level detector. A decrease in magnet current is accomplished by a proportional decrease in signal voltage at pin 2 of the level detector and any decrease of signal voltage below the applied reference voltage level causes saturation of the level detector's output transistor. The transistor thus completes a path for the application of +28 vdc power through pin 10 of the level detector, pins E of connector J3 and A of connector P27 (sheet 5), to pin B1-2 of latch circuit No. 3. The applied positive signal fires and SCR within the latch circuit module, and the SCR applies +28 vdc to illuminate LOW MAGNET CURRENT indicator lamp DS16 (red). The +28 vdc output at pin B2-8 energizes protective circuit relay K20 sheet 6) which, in turn, applies +28 vdc through connector pins J2-q and P35-u and RF1 filter FL7B4 in the primary power distribution panel to energize relay K3. When energized, relay K3 applies +28 vdc to illuminate (red) the top half of split-lens indicator A1 XMIT FAULT) and applies +28 vdc through pins C2 and C1 of ALARM DIS-ABLE switch A1 to the positive terminal of buzzer DS11. When set to ALARM DIS-ABLE position, switch A1 removes power from buzzer DS11 and applies +28 vdc to illuminate (red) the bottom half of split-lens indicator A1 (ALARM DISABLE).

b. Level detector AR1 (sheet 4), generates a positive signal when it senses a high body current condition. A +1 vdc reference voltage level derived at the junction of resistors R4 and R6 is applied in pin 2 of level detector AR1. When body current is present, a small voltage is developed at the junction of resistors R1 and R2 and applied through resistor R3 to pin 3 of level detector AR1. Any increase of voltage at pin 3 results in a fault signal (positive output) at pin 10 which is applied o pin B1-4 of latch circuit No. 3. Within the latch circuit module, the fault signal fires an SCR which simultaneously applies +28 vdc to three circuits:

(1) An output at latch circuit pin B4-5 illuminates HIGH BODY CURRENT indicator lamp DS17 (red).

(2) An output at pin B2-8 energizes protective circuit relay K20, illuminates XMIT FAULT indicator lamp A1, and turns on the audible alarm (buzzer DS11) is described in a above.

(3) An output at pin B5-10 energizes vacuum switch S1 which diverts beam power to chassis-ground while the beam power interlock is being disengaged by protective circuits relay K20.

c. Level detector AR3 generates a positive signal when it senses a high beam current condition. The beam current develops a negative voltage across resistor R3, and resistor R11 couples the small negative voltage from resistor R3 to pin 4 of level detector AR3. A negative reference voltage, derived at the wiper arm of potentiometer R15, is also applied to pin 3 of level detector AR3. The reference voltage is adjustable over a range of 0.0 to-2.74 vdc, however, it is set during equipment alignment for-0.90 vdc trip point level. When the voltage at pin 4 of level detector AR3 goes more

negative than-0.90 vdc, pin 10 goes positive to signify a fault. This positive signal is applied through pins 12 and z of connector J1 of pin C of connector P27 (sheet 5) to pin B1-5 of latch circuit No. 3. Within the latch circuit module, the positive signal fires an SCR which applies +28 vdc to illuminate HIGH BEAM CURRENT indicator lamp DS18 (red), energize protective circuit relay K20, illuminate XMIT FAULT indicator lamp A1 (white), and turn on the audible alarm as described in *a* above.

2-30. Klystron and Isolator High Vswr Detection
(fig. FO 2-1, sheet 13 and Fig. FO 2-4, sheets 4 and 5)

Electrically identical fault circuits detect high vswr conditions at two points in the high-power segment of the transmitting circuits by comparing forward and reverse power sample levels. Each fault circuit initiates and holds illuminated indications, circuit inhibits, and an audible alarm when the reverse power sample applied to the circuit exceeds an acceptable limit.

a. The klystron high vswr detect circuit receives rf power sample from the reverse sample part of directional coupler DC3 (fig. FO 2-1, sheet 13). Waveguide-to-coaxial adapter CP6 applies the rf power sample to low-pass filter FL5 which passes the transmit band frequencies and attenuates their harmonics 50 dB. Rf detector A7 receives the filtered rf sample and removes the negative portions to provide a varying-level positive dc input signal to detector amplifier (vswr) A10 (fig. FO 2-4, sheet 4). Within the detection amplifier, the reverse power signal level is developed across resistors R1, R2, and R6, and coupled by resistor R4 to pin 3 of the dc amplifier. A reference voltage level of approximately-6.5 vdc is applied at pin A1-2. The reference voltage is derived from the voltage divider network consisting of resistors R3 and R5, diodes CR1 and CR3, and a 1-kilohm resistor in an isolator comparator module. The response of detector amplifier A10 is set by the use of selected-value components during manufacture to provide a positive output at pin 10 of the dc amplifier when a maximum acceptable positive level is exceeded at pin 3. Thus, when the re verse power sample level increases due to high VSWR, pin 10 of the dc amplifier goes positive. The positive signal is applied through pins F and J of connector J2 and P27, respectively (fig. FO 2-4, sheet 5) to pin C1-5 of latch circuit No. 2. Within latch circuit No. 2, the positive signal fires an SCR which applies +28 vdc (through reset circuits) to three separate circuits:

(1) A +28 vdc output at pin D5-8 illuminates HIGH VSWR KLYSTRON indicator lamp DS13 (red).

(2) A +28 vdc output at pin D4-2 operates diode switch trigger circuit A9, and the diode switch trigger circuit attenuates klystron drive power by 40 db.

(3) A +28 vdc output at pin D5-10 energizes protective circuit relay K20, illuminates XMIT FAULT indicator lamp Al (white), and turns on the audible alarm.

b. The isolator high vswr detect circuit operates similar to the klystron high vswr detect circuit described in a above. Directional coupler DC5 (fig. FO 2-1, sheet 13) provides an isolator reverse power sample at its reverse power port. The rf sample is processed through waveguide-to-coax adapter CP5, low-pass filter FL9, and rf detector A5. The filtered and detected reverse power signal is then applied to detector amplifier (vswr) A11 (fig. FO 2-4, sheet 4). When the detector amplifier senses a high vswr condition, it generates a positive signal that fires an SCR in latch circuit No. 2 (fig. FO 2-4, sheet 5). Three +28 vdc power outputs are simultaneously applied to separate circuits in the same manner as described in a above and the results obtained are the same, except HIGH VSWR ISOLATOR indicator lamp DS14 (red) illuminates.

2-31. Klystron Waveguide Arc Detection
(fig. FO 2-4, sheet 4)

a. Arc detector amplifier A13 detects arcing that may occur in the klystron electron tube or its output port and waveguide. The arc detector amplifier is oriented on a waveguide adapter so that its photodiode CR2 is directly exposed to light from arcs. Photodiode CR2 is a junction-barrier device used as a photovoltaic cell. Connected in parallel across resistor R3, the photodiode is reverse-biased approximately 2 volts and only barrier leakage current flows in an insignificant amount under dark (no-arc) conditions. When an arc occurs, the light striking the photodiode's reverse-biased junction produces an increase current flow across the junction. Effectively, the resistance decreases as the light increases and the voltage at dc amplifier pin 3 rises.

b. Upon the occurrence of an arc in the klystron, the voltage at pin 3 rises sufficiently to overcome the effects of a reference voltage applied at pin 2, and pin 10 goes positive. This waveguide arc fault signal is applied to input pin D1-4 of latch circuit No. 2. Within latch

circuit No. 2, the fault signal fires an SCR that simultaneously applied +28 vdc (through reset circuits) to:

(1) Illuminate WG ARC KLYSTRON indicator lamp DS15 (red).

(2) Enable diode switch trigger circuit A9 which attenuates klystron drive power by 40 db.

(3) Energize protective circuit relay K20 and illuminate XMIT FAULT indicator lamp A1 (white).

(4) Turn on the audible alarm.

c. A voltage divider consisting of resistors R4 and potentiometer R5, applies the positive reference voltage to dc amplifier pin 2 in arc detector amplifier A13. Potentiometer R5 of the voltage divider network is the level-set adjustment control for the reference voltage.

2-32. Isolator Waveguide Arc Detection
(fig. FO 2-4)

a. A component circuit monitors rf power levels at two points in the high-power segment of the transmitting circuits. The comparator circuit detects power level reversals incurred by waveguide arcing, and generates a fault signal. A sample representing isolator rf power output is obtained at the forward power sample port of directional coupler DC5 (fig. FO 2-1, sheet 13). The rf power sample is processed through variable attenuator AT15, waveguide-to-coaxial adapter CP8, and low-pass filter FL4. Filter FL4 allows transmit band frequencies to pass unimpeded while attenuating their harmonics 50 db. Frequency detector A6 converts the rf sample to a varying-level positive dc signal and applies it through coaxial cable W10 to connector J1 of detector amplifier (vswr) A9 (sheet 4). Within detector amplifier A9, the isolator forward t power signal is developed across the resistor network of R1, R2, and R6, and is coupled by resistor R4 to pin 3 of the dc amplifier. A reference voltage level of approximately-6.5 vdc is applied at pin 2 of the dc amplifier. The dc amplifier produces a positive output at pin 10 as long as the positive dc signal at pin 3 remains at or above a minimum acceptable level.

b. Arcing within the rf reflection isolator is accomplished by a drop in forward power, an abnormal decrease in voltage level applied to (pin 3 of the dc amplifier, and loss of the positive output at pin 10. The signal output of the dc amplifier is applied through connector pins J2-F and P27-D (sheet 5) to input pin B10-9 of isolator arc sensing circuit A8. Concurrently, a positive signal that represents klystron forward power is applied from pin C6-4 of low rf sensing circuit A6 to pin B6-4 of isolator arc sensing circuit A8. A dc amplifier within the isolator arc sensing circuit constantly monitors the two forward power signals and remains in a quiescent ate as long as the isolator power signal is more positive than the klystron power signal. If arc occurs in the isolator, the associated forward power signal decreases below the level of the klystron forward power signal, and the dc amplifier generates a positive signal to pin C1-4 latch circuit No. 2 to fire an SCR. The SCR simultaneously applies +28 vdc power through .set circuits to illuminate WG ARC ISOLATOR indicator lamp DS12 (red), operate diode switch trigger circuit A9 to attenuate klystron drive power by 40 db, energize protective circuit relay 20, illuminate XMIT FAULT indicator lamp 1 (white), and turn on the audible alarm as described in paragraph 2-29*c*.

2-33. Diode Switch Trigger Circuits
(fig. FO 2-1, sheet 12 and fig. FO 2-4, sheet 5)

a. Diode switch trigger circuit (A9) (fig. FO 2-4) controls the application of the rf drive to the twt and power amplification circuits. The complete switch trigger circuit consists of diode switch trigger circuit (A9) resistor R3, and conducts of fault circuit reset switch S4.

b. Under normal transmit operation, diode switch trigger circuit (A9) presents an open condition in the triggering circuit which applies 28 vdc bias through J3 and cable W29 to rf switch S6 on transmitter plate assembly A3A10 (fig. FO 2-1). The positive bias holds the witch in the on condition, and the rf drive signal is coupled through to the twt. When a fault is detected in the high power segment of the transmit circuit, the control voltage (+28 vdc) shifts to approximately-21 vdc. This negative as holds the switch in the off condition and attenuates the rf drive by 40 db.

2-34. FAULT Lamp and Audible Alarm Circuit Operation
(fig. FO 2-4, sheet 6)

Operating faults that could conceivably result equipment damage if prolonged turn on audible alarms and illuminate of XMIT FAULT indicator, and provide high and low rf power conditions in the shelter. Additionally, high-power and high voltage faults that could cause equipment damage energize a protective circuit relay and produce visible and audible fault indications.

a. Regardless of fault signal origin, +28 vdc is applied to energize fault relay K3. Relay contacts B2 and B1 apply +28 vdc unregulated power to illuminate

(white) the XMIT FAULT indicator, which is the top half of split-lens indicator switch A1, and to audible alarm buzzer DS11. The audible alarm can be inhibited by setting switch A1 to the ALARM DIS-ABLE position, thus opening the +28 vdc power path to the buzzer. At the same time the buzzer is disabled, by means of the opened switch contacts, +28 vdc is applied through the alternate action of switch A1 to illuminate (white) the ALARM DISABLE indicator which is the bottom half of split-lens indicator switch A1. Elimination of the fault indication can be accomplished either by correcting the malfunction or by reset action at transmitter control panel.

b. Transmit interlock, body and magnet flow, and high coolant temperature fault signals are applied from latch circuit module pins A2-E10-9 and A4-D10-9, through pins J1-Y, P28-Y and P28-q and RFI filter FL7-B4 in primary power panel A14 to energize fault relay K3, which in turn, applies power to illuminate XMIT FAULT indicator lamp A1 (white) and turn on buzzer DS11.

c. Coolant flow faults deenergize flow switch relay K19. With flow switch relay K19 deenergized, contacts B2 and B3 make and apply +28 vdc to relay K3. Relay K3 energizes and illuminates XMIT FAULT indicator lamp A1 (white) and initiates buzzer DS11.

d. High and low current, high vswr, and waveguide arc fault signals are applied from the latch circuit modules to relay K3. Relay K20 contacts A2 and A1 make and apply +28 vdc regulated power, through the same route as in c above, to relay K3. The B-section contacts of relay K3 perform an interlock function.

e. On-line transmitter output power assembly 1A2A27A4 contains both low and high power adjustable fault limits which operate in conjunction with the transmitter forward power sampled output. The forward power sampled output is fed to the rf power meter assembly as described in paragraph 2-17*d*. When the transmitter output power rises or falls below the operator established limits, an audible alarm is activated.

2-35. Fault Reset Circuit Operation
(fig. FO 2-4, sheets 5 and 6)

Two reset switches provide a means for locally or remotely interrupting latched fault circuit power. The local and remote switches are located at the antenna pedestal and in the shelter, respectively. Minor fault circuits (amber indicators) are not latched; the more significant fault circuits (red indicators) are latched, and the indicators remain illuminated until power is removed or a reset switch is momentarily set to its RESET position. Since the fault indicators receive + 28 vdc power through an SCR or contacts of a latched relay, interruption of the power by means of a reset switch terminates the indication.

a. The +28 vdc power for the 15 fault indicators is applied through two RESET switches and individual SCR's within six latch circuit nodules on the transmitter control panel. Power applied at each input pin of the latch circuit module is branched to the anodes of SCR's within the latch circuit. When a fault is detected and its associated fault signal fires one of the SCR's, the SCR conducts and illuminates a fault indicator. The indicator can be extinguished only by shutting down equipment power or momentarily operating one of the two reset switches to interrupt the current flow. With current flow interrupted, the SCR reverts to a nonconducting state.

b. Upon detection of a transmit fault, relay K3 energizes and its B-section contacts initiate visual and audible fault indications, and its A-section contacts latch the relay as described in paragraph 2-34. When the reset switch S4 is momentarily opened, it removes the +28 vdc regulated power path to the coil of relay K3, and consequently the regulated power path to XMIT FAULT indicator lamp Al and audible alarm buzzer DS11.

c. Diode switch trigger circuit A9 also has an SCR that latches in the conduction state when a high voltage or high-power fault is detected. When fired by a fault signal, the SCR applies a negative biasing voltage through pin A5-8, connector pins J2-r and P35-CC, and RFI filter FL14A2, to RESET switch S4. With switch S4 normally closed, the negative biasing voltage is applied through contact C2, RFI filter FL14A3, connector pins J8-DD and P27-V, and TB1 pin 12 to resistor R3. Diode switch trigger circuit A9 can be reset by momentarily opening the reset switch to interrupt SCR current flow.

2-36. Klystron Body, Beam, and Magnet Current Faults Test Circuit
(fig. FO 2-4, sheet 4)

When set to FAULT TEST, switch S7 simulates high or low current faults by basically applying or removing voltages.

a. The A-section contacts of FAULT TEST switch S7 break the magnet low current. sensing path between shunt resistor R3 and level detector A1. With the applied voltage removed, the level at pin 2 of level detector A1 drops to zero. Level detector A1 senses the decrease below the reference level and generates a fault signal.

b. The B-section of FAULT TEST switch S7, apply-28 vdc through connector pins J2-f, P24-h, and P1-4 to the anode of Zener diode CR2. Zener diode CR2 drops 10 vdc, thus applying-18 vdc across the resistor network of resistors R17, R10, and R16. Resistor R17 limits current passed by the Zener diode, while resistors R10 and R16 divide the voltage to apply a-2.1 vdc level to pin 3 of dc amplifier AR2. Normally pin 3 remains more positive (zero level) than pin 2 resulting in a positive

output at pin 10. However, when test voltage is applied at pin 3, it becomes more negative, and the output at pin 10 also goes negative. Resistor R12 couples the negative signal to pin 4 of level detector AR3 and the negative signal trips the level detector in the same manner as a high beam current level fault signal.

c. The C-section contacts of FAULT TEST switch S7 apply vdc regulated power through connector pins J2-MM, P24-g, P1-6, and resistor R1. Resistors R1 and R5 decrease the voltage applied through diode CR3. The resulting positive signal, coupled to level detector AR1 by resistor R3, exceeds the positive reference level (at pin 2), and level detector AR1 generates a fault signal as described in paragraph 2-29.

2-37. High Vswr and Arc Faults Test Circuits
(fig. FO 2-4)

Switch S6 (sheet 4) connects +28 vdc-regulated power to simulate high vswr conditions when set to VSWR TEST and simulates waveguide arcing conditions when set to ARC TEST.

a. In the VSWR TEST position, switch S6 contacts 5 and 4 apply +28 vdc through connector pins J2-P and P45-H to Zener diode CR2, and also through connector pins J2-T and P44-H to Zener diode CR2. Each Zener diode drops 10 vdc, thus applying +18 vdc to its associated resistor network of resistors R1, R2, and R6. Resistor R4 in each detector amplifier (vswr) couples the simulated fault signal to pin 3 and the amplifiers operate as described above, for actual faults.

b. In the ARC TEST position, switch S6 applies +28 vdc regulated power to two separate points:

(1) Through connector pins J2-NN and P42-H to illuminate lamp DS1. The lamp is confined in a drilled chamber and its light rays reflect off the chamber walls and through a milled passage onto photodiode CR2. Conduction of the photodiode increases and the arc detector initiates a fault signal for actual klystron arcing.

(2) Applied to input pin B10-8 of isolator power comparator A8 (sheet 5), the +28 vdc represents a significant increase in klystron forward power. The simulated rise in klystron power affects a dc amplifier within isolator power comparator A8 in the same manner as an abnormal drop in isolator power. Thus, a waveguide arcing condition is artificially produced, and the fault detect circuit operates as described in paragraph 2-31.

2-38. Fault and Status Indicator Test Circuits
(fig. FO 2-4)

All indicators on the transmitter control panel of the AN/TSC-54 can be simultaneously tested by means of LAMP TEST switch S3. Three contact sections of witch S3 complete current paths through all the indicator lamps when the switch is momentarily set to AMP TEST.

a. A-section contacts of LAMP TEST switch S3 apply +28 vdc regulated power through diodes to indicator lamps that are not controlled by latch circuits. For example, power applied through diode CR1 illuminates LOW LIQUID WARNING indicator lamp DS1 amber) Diode CR1 blocks current passage to the other indicators when a fault signal illuminates the LOW LIQUID WARNING indicator lamp. The A-section contacts also connect the +28 vdc unregulated power to a lamp test buss that distributes the power through he diodes to various transmit function status indicator lamps (sheet 2).

b. B-section contacts of LAMP TEST switch S3 (sheet 5) apply + 28 vdc regulated power for testing fault indicators controlled by latch circuits. The power applied at one input pin of a latch circuit module is ranched through diodes to each of the fault indicators controlled by the latch circuit module. For example, 28 vdc power is routed from LAMP TEST switch S3 contact B3 through connector pin P1-A6-10/5 (sheet) to pin E10-7 of latch circuit No. 4. The outputs from pins E9-3, E9-5, and E9-1 of latch circuit No. 4, are simultaneously applied to INTERLOCK indicator amp DS19, INTERLOCK indicator lamp DS7, and LOW LIQUID indicator lamp DS20. Diodes within the latch circuit module restrict fault signals to their respective fault indicators.

c. C-section contacts of LAMP TEST switch S3 (sheet 5) complete a current return path for LOW RF OWER indicator lamp DS11 (white). The +28 vdc regulated power is applied through indicator lamp S11 pins 1 and 2, pin C7-8 of low rf sensing circuit 6, a diode within the sensing circuit module, and pin 7-6 to contact C3 of LAMP TEST switch S3. While AMP TEST switch S3 is held in the LAMP TEST position, the C-section contacts complete a current path to the common terminal on the +28 vdc regulated power supply.

2-39. Power Switching and Protective Interlock Circuits
(fig. FO 2-4)

Complete transmitter power turn-on is controlled by a sequential series of switch and relay contact actions at apply the necessary input power to operating motors and power supplies.

a. Functionally identical switches are provided for transmitter power turn-on at either the antenna pedestal or the equipment shelter. The active control point is determined by the setting CONTROL key lock ditch S2. In the PEDESTAL position, switch S2 applies +28 vdc

unregulated power through RFI filter FL6A4 to relay K11. The relay energizes and close contacts A1 and A2 (sheet 2). In the LOCAL position switch S2 disconnects the +28 vdc power from relax K1 causing relay K11 to deenergize and close contacts A2 and A3. Relay contacts A1 and A2 open to insert pedestal XMIT POWER control switch S12 into the interlock circuit, while contacts A2 and A3 insert shelter TRANSMITTER POWER control switch S1 into the interlock circuit.

b. Neither POWER control switch (*a* above) can initiate power turn-on unless low liquid interlock relay K17 (sheet 3) is energized. Relay K17 is controlled by a low liquid interlock switch in heat exchanger A3. As long as the liquid coolant supply remains above a mini mum acceptable level, the interlock switch remains closed and relay K17 is energized. The B-section contacts of relay K17 connect +28 vdc unregulated power through connector pins J2-n, and P26-s to XMIT POWER switch S12. Since contacts 2 and 1 of XMIT POWER switch S12 are normally closed, the +28 vdc unregulated power is applied through connector pins J2-KK and P36-p, and filter FL5B1, to contact 6 of TRANSMITTER POWER switch S1.

c. Assuming that CONTROL keylock switch S2 (*a* above) is set to PEDESTAL, the transmit power turn on sequence in initiated by momentarily setting XMIT POWER switch S12 to ON. For a brief moment, contacts 5 and 4 of switch S12 apply +28 vdc through connector pins J2-t and P28-DD (sheet 2) to pedestal control relay K11. Since the relay is energized, the +28 vdc is applied to body and magnet flow relay K18 and blower motor interlock relay K14. Relay K14 initiates filament power turn-on (*e* below) and a 9-minute delay sequence (*f* below). The +28 vdc performing the actual initiate function is applied through connector pins J2-Y and P24-L to heat exchanger contactor relay K2. Relay K2 energizes and contacts 12 and 11 make to complete a current path that latches the contactor in its energized state. Latching power is received through connector pins J1-M and P35-P (sheet 1), RFI filter FL6C4, normally-closed contacts 5 and 6 of TRANSMITTER POWER switch S1, RFI filter FL5B1, connector pins J9-p and P27-KK, and normally-closed contacts 1 and 2 of XMIT POWER switch S12.

d. Assuming that CONTROL keylock switch S2 (*a* above) is set to LOCAL, transmit power turn on is initiated by momentarily setting TRANSMITTER POWER switch S1 to ON and completing a +28 vdc power path to the A-section contacts of pedestal control relay K11 (sheet 2). Since relay K11 is deenergized, its contacts A3 and A2 are closed, and +28 vdc power is applied to energize and then latch heat exchange contactor K2 as described in paragraph 2-40.

2-40. Progressive Application of Operating Power

(fig. FO 2-4)

Operation and latching of heat exchanger contactor K2 starts a series of actions that includes application of operating power to various functional units and timing of circuit warmup periods.

a. First, the A, B, and C sections of contactor (fig. FO 2-7, sheet 3) apply phase A, B, C power to transmitter liquid cooler A3. Also, phase A and C power is applied by relay K1 to liquid coolant heater HR1. Transmitter liquid cooler A3 is activated into circulating liquid coolant through the microwave section cooling system.

b. The +28 vdc power, now available at pedestal control relay K11 (sheet 2), energizes relays K4 and K12. The A and B sections of relay K4 (fig. FO 2-7, sheets 3 and 8) connect phase C power to RF amplifier A14, while A and B sections of relay K12 connect phase C power to klystron blower motor B5. With power applied, the rf amplifier and the klystron blower start operating.

c. When the liquid coolant flow through the klystron and electromagnet increases sufficiently to close body and magnet flow switch S3, relay K18 energizes. Contacts B1 and B2 of relay K18 (sheet 2) make and apply +28 vdc power through connector pins J2-r and P24-J to magnet power supply contactor relay K3. Relay K3 energizes and its contacts 11 and 12 make to initiate preheat status indications as described in paragraph 2-43. Concurrently, the A, B, and C sections of relay K3 apply phase A, B, and C power to magnet power supply A21.

d. Meanwhile, when the klystron cooling air motion reaches sufficient velocity to close blower motor interlock switch S5 (sheet 2), the switch applies +28 vdc unregulated power from relay K17 (sheet 1) through connector pin J2-p, terminals 3 and 4 of terminal board TB5, and connector pin P28-t to energize relays K14 and K8.

e. With blower motor interlock relay K14 energized contacts A1 and A2, and B1 and B2 make, and simultaneously remove illuminating power from FILAMENT COOLING indicator lamp DS24 (red) and apply operating power to delay relays (para 2-4), and to filament power relay K13. Filament power relay K13 energizes, and its A-section contacts (fig. FO 2-7, sheet 3) apply phase C power to the klystron filament control transformer in high voltage cage A11. For approximately 1 minute, the A-section contacts of the relay apply the phase C power through surge resistor R5, which is in series with the klystron filament control transformer, and then contacts B1 and B2 of relay K7 make and bypass the surge resistor.

f. Relay K8 (sheet 2) holds for 60 seconds after power

is applied to its coil (e above) and then its A and B sections (sheet 4) make. The hold-and-make action provides a 60-second delay before applying +28 and-28 vdc power to magnet power supply A21.

2-41. Beam Power Delay
(fig. FO 2-4, sheet 2)

The beam power supply cannot receive its operating power until a series of time delays provided by relays is satisfied. Application of +28 vdc to relay K6 and relay K7 does not cause an immediate switching action. Relay K6 remains deenergized during its 1-minute delay and then energizes. Since contacts 8 and 6 of relay K6 break and short the coil of relay K7, it too remains deenergized for 1 minute. This holding action prevents damage from a current surge to the klystron filament control transformer by initially applying power through a surge resistor. When relay K6 energizes, contacts 8 and 6 break and remove the short from the coil of relay K7 and relay K7 energizes. The B-section contacts of relay K7 now bypass the surge resistor, while contacts A2 and A1 apply +28 vdc to relays K15, K24, and K16. Although the power is simultaneously applied to the three relays, the latter two relays cannot operate since their coils are shorted by the closed contacts of the preceding relay. After a 4-minute time delay provided by relay K15, it operates and connects the coil of relay K24 to the 28 vdc unregulated power return line. Four minutes later, relay K24 operates and connects the coil of relay K16 to the return line, and relay K16 energizes. Operation of relay K24 completes the 9-minute delay period and makes possible the application of beam power; however, this is contingent on the satisfactory closure of contacts in all subsequent protect relays. To prevent turn on surge and the surge associated with the crowbar function when a fault is detected, solid state contactors (K1, 0A, K2, 0B and K3, 0C) are connected in series with mechanical contactors which are parallelled with starting resistors R1, R2, and R3. When a power-on command is received, the solid state contactors close much faster (approximately 100 ms) before the slower mechanical contactors thereby applying power through the starting resistors. Approximately 100 ms later, the mechanical contactors close, shorts out the starting resistors, and full power is applied to the beam supply. When a fault is detected, the solid state contactors open very fast and power is removed from he beam power supply.

2-42. Radiation Hazard Warning
(fig. FO 2-4, sheet 2)

The radiation hazard warning provides a 120 vac circuit closure to pedestal bulkhead connector J1 only when beam power is on from either the HPA or LPA. With HPA beam power applied, +28 vdc unregulated power from the anode of diode CR11 is routed through he contacts of relay K101, J1-*c*-P26, P76-C-J1 and energizes relay A26K1. The resultant relay contact closure between A1 and A2 applies 120 vac from TB3-13 to bulkhead connector J1-A. This 120 vac can be used to illuminate a radiation hazard warning accessory indicating that beam power is on. When the system is in the dummy load configuration, +28 vdc unregulated power from the anode of diode CR14 energizes relay 2A3A7K101 and breaks relay contacts A2-A3. The +28 vdc to relay A26K1 is removed, the relay is deenergized and the 120 vac (radiation hazard warning) loop to bulkhead connector J1 is opened. Similarly, when LPA beam power is on, a low level signal generated by the LPA is sent to relay 2A3A26K2 through connector P76 pin E; power for the relay (at 76 pin F) is derived from the LPA. When energized, relay contacts A1-A2 close. These contacts are connected in parallel with the A2-A1 contacts of relay 1, and perform the function described above.

2-43. Preheat Status Indications
(fig. FO 2-4, sheet 2)

Since preheat standby relay K16 remained deenergized during the delay period (para 2-41), its contacts A2 and A3 remain closed and apply +28 vdc to illuminate PREHEAT indicator lamp DS5 (white). The indicator driving power is applied through contacts B1 and B2 of relay K18, connector pins J2-r and P24-J, contacts 11 and 12 of contactor relay K3, connector pins J1-K and P28-s, contacts A2 and A3 of relay K16, and connector pins J2-AA arid P26-t to a branching point at the anode of diode CR7. For a preheat status indication at the antenna pedestal, the diode applies the +28 vdc power directly to PREHEAT indicator lamp DS5 (white). For a preheat status indication in the equipment shelter, the +28 vdc power is applied from the anode of diode CR7 through connector pins J2-b and P36-s, and filter FL5B4, to PREHEAT indicator lamp DS3 (white). Both PREHEAT indicators remain illuminated during the 9-minute delay that provides for circuit warmup and stabilization. The indicators extinguish as relay K16 energizes and completes an interlock circuit for the beam power supply control switches.

2-44. Protective Circuits Interlocks
(fig. FO 2-4, sheet 2)

Following the energizing of preheat standby relay K16, continuity of the control power path to the beam power switches is determined by the operation of various protective circuit relays.

a. The +28 vdc is applied through the relay interlock circuit from preheat standby relay K16 to flow switches relay K19. Flow switches relay K19 energizes when a satisfactory coolant flow is achieved through the waveguide components, dummy load, and klystron collector coolant jackets.

b. Protective circuits relay K20 must be deenergized to continue the application of control power. Relay K20 is deenergized if the klystron and electromagnet high and low currents are within limits, VSWR is below maximum acceptable limits, and no arcing is occurring within the waveguides.

c. System coolant high temperature relay K21 must be energized to continue the application of control power. Relay K21 remains energized provided the AN/TSC-54 system coolant temperature remains below a maximum limit.

d. Alternate paths are provided for further application of control power to the beam power switches. Individual switches in waveguide switch S3 determine the active path. With waveguide switch S3 set to dummy load, the +28 vdc control power is applied through connector pins J2-Y and P22-C, the closed contacts of the load switch and connector pins J4-D and P26-P to the cathode junction of diodes CR13 and CR14. Diode CR13 completes a current path to illuminate DUMMY LOAD indicator lamp DS8 (red) and diode CR14 completes a current path for the application of power to interlock relay K5.

e. When waveguide switch S3 is set to the antenna position, the load switch contacts open and the antenna switch contacts close. Thus, the control power is diverted through sector limit relay K2 to interlock relay K5.

f. Interlock relay K5 provides the final contact closure required for the application of control power to the beam power switches. Relay K5 energizes when all mechanical interlocks are secured. BEAM POWER switches S13 and S4 are electrically identical and either switch may be used to turn on beam power; however, the B-section contacts of pedestal control relay K11 must be positioned to correspond with the BEAM POWER switch selected for beam power turn-on. The B-section contacts of the relay selectively insert the BEAM POWER switches into the circuit just as the A-section contacts insert the POWER switches (para 2-39). BEAM POWER switches S13 and S4 cannot turn on beam power when RESET switch S4 is held in the RESET position. This action provides protection to the klystron.

2-45. Beam Power Turn-on
(fig. FO 2-4, sheet 2)

a. Assuming that the CONTROL keylock switch is set to PEDESTAL, beam power turn-on is effected by momentarily setting BEAM POWER switch S13 to ON. With switch S13 set to ON, contacts 5 and 4 make and apply +28 vdc through connector pins J2-X and P28-w, closed contacts B1 and B2 of pedestal control relay K11, and connector pins J2-KK and P24-N to energize beam power supply contactor relay K1. With relay K1 energized, contacts 11 and 12 make, and complete a current path that latches the contactor in its energized state by connecting +28 vdc power through an alternate route from contact 2 of BEAM POWER switch S13, pedestal RESET switch closed contacts S4-C1 and C2, and connector pins J2-JJ and P24-U. With RESET switch S4 forcibly held in the RESET position, the +28 vdc path from S13-2 will remain open and relay K1 will not energize. Concurrently, the A, B, and C sections of contactor relay K1, apply phase A, B, and C power to

power supply assembly 2A2 through solid state contactors K1 and K2, and surge protection resistors R11, R12, and R13, respectively. Turn on of beam power completes the sequential application of operating power for transmit operation of the AN/TSC-54.

b. Assuming that CONTROL keylock switch S2 is set to LOCAL, beam power turn on is effected by momentarily setting BEAM POWER switch S4 to ON. Contacts 2 and 3 of BEAM POWER switch S4 make and apply +28 vdc control panel through RFI filter FL7B3, and connector pins J8-t and P28-v to relay K11. Since pedestal control relay K11 is deenergized for the shelter control of power, relay K11 applies the control power through connector pins J2-KK and P24-N to beam power supply contactor relay K1. The contactor relay then applies operating power to the klystron beam power supply as described in a above. BEAM POWER switch S4 is connected with BEAM POWER switch S13 through connector pin J1-Y, filter FL6B3 and connection pins J11-Y and J1-DD. If RESET switch S4 is held in the RESET position, the 28 vdc path is interrupted and relay K1 cannot be energized by placing BEAM POWER switch S4 to the ON position.

2-46. Standby/Transmit Indications
(fig. FO 2-4)

Standby and transmit indications are duplicated at the antenna pedestal and in the shelter to allow operator personnel to monitor transmitter status at either position.

a. Following normal relay delays, and operation of all interlocks that control power to the BEAM POWER switches, the STANDBY indicators are illuminated. Indicator power, available at BEAM POWER switch S13 (sheet 2) is applied through RESET switch contacts S4-C1 and C2, connector pins J2-JJ and P24-U to beam power supply contactor relay K1. Since the contactor is still in its deenergized state and contacts 14 and 13 are closed, the indicator driving power is applied through connector pins J1-P and P26-d to a branching point at the anode of diode CR9. Diode CR9 applies power to STANDBY indicator lamp DS6 (blue). At the same time, the power is applied from the branching point through connector pins J2-d and P26-t, and RFI filter FL5C1, to STANDBY indicator lamp DS4 (blue). Both indicators illuminate and remain illuminated provided that all circuit interlocks remain closed and beam power supply contactor relay K1 remains deenergized. When any interlock opens due to a fault, or the contactor operates, indicator power is interrupted and both STANDBY indicators extinguish.

b. When beam power supply contactor relay K1 energizes, contacts 12 and 11 make; relay K1 latches and applies power through connector pins J1-N, P29-KK, J2-h, and P26-Z to a branching point. From this branching point, diode CR11 applies power to TRANSMIT indicator amp DS7 (green). At the same time, the power is applied from the branching point through connector pins J2-e and P26-x and RFI filter FL5C4, to XMIT indicator lamp DS5 (green). Both indicators illuminate and remain illuminated provided that beam power supply contactor relay K1 remains energized. Placing RESET switch S4 to RESET resets latch circuits A1, A2, and A4 (sheet 6) and both indicators will extinguish.

2-47. Transmit Power Turnoff
(fig. FO 2-4, sheet 2)

Transmit power is normally turned off by momentarily setting either the XMTR ON toggle switch on the rf power monitor and control panel or the XMIT POWER ON-OFF toggle switch on the transmitter control panel to the down position, to OFF. With latching power interrupted, all contactors in the interlock circuit deenergize and remove operating power from heir associated power supplies. Transmit power can also be automatically turned off to protect he equipment when the liquid coolant supply is below a minimum level. Upon occurrence and detection of this fault condition, low liquid interlock relay K17 deenergizes and interrupts the latching power. Once turned off, transmit power cannot be fully restored until another 9-minute warmup period, provided by the delay relays, is satisfied.

2-48. Beam Power Turnoff
(fig. FO 2-4)

Beam power is normally turned off by momentarily setting either the BEAM ON toggle switch on the power monitor and control panel 1A2A27 (sheet 2) or the BEAM POWER ON-OFF toggle switch on the transmitter control to OFF. Beam power is also turned off if RESET switch S4 (sheet 5) is held in the RESET position. This action interrupts the latching power to the beam power supply contactor. The contactor deenergizes and provides STANDBY indications. Following a normal turnoff, the beam power can be immediately restored as described in paragraphs 2-44 and 2-45. Beam power can also be automatically turned off by any operational fault that could damage the equipment. Satisfactory

operating conditions are represented by relay contact closures; while unacceptable conditions (faults) are represented by opened relay contacts. Opening of any one set of the series-connected protective circuit relay contacts interrupts the latching power applied to the beam power supply contactor and operating power is removed from the klystron beam power supply. The STANDBY indicators do not illuminate after a fault-initiated turn off until all contactor and relay contact closures are again completed.

Section III. RECEIVING FUNCTION

2-49. General

a. This section contains a functional analysis of the receiving circuits of Satellite Communication Terminal AN/TSC-54. In the receive direction, the terminal is capable of receiving multiple channel signals in the frequency range of 7.25 to 7.75-GHz. The signals are processed, separated, and applied to the terminal user, external user, or retransmitted to another satellite as applicable.

b. A functional analysis of the rf components is covered in paragraphs 2-50 through 2-56. Paragraphs 2-57 and 2-58 cover the communication demodulator and the beacon demodulator. The operation of the baseband circuits is given in paragraphs 2-59 through 2-65. The functional analysis of the OBN. monitor panel is given in paragraph 2-65.1.

2-50. General Analysis of Microwave Signal Reception

a. Microwave signal originating at a satellite impinge on adjoining quadrants of the AN/TSC54 antenna reflector. Each reflector quadrant converges the received energy onto a DIELGUIDE assembly subreflector mounted at its focal point and the subreflector redirects the energy into its associated waveguide feed assembly.

b. Each waveguide feed assembly consists of a feed horn, polarizer, and a duplexer. The feed horn converges received energy directly to the input port of the polarizer in a circularly polarized mode. Five pairs of iris plates within the polarizer change the signal energy polarization from circular to linear for application to the duplexer. The duplexer couples the receive signal to a rectangular waveguide section. The four portions of the polarized receive signal are applied from the waveguide feed assemblies to waveguide tees for comparison.

2-51. Tracking Error Development Circuits
(fig. FO 2-2, sheet 3)

a. The comparator network of the AN/TSC-54 consists of waveguide tees A20, A21, A22, and A23. To simplify discussion, the four received signal portions are designated A, B, C, and D, and are derived from similarly identified DIELGUIDE assemblies. A and C signals applied to waveguide tee A22 and an A minus C signal to waveguide tee A23. Concurrently, B and D signals to waveguide tee A21 produce a B plus D signal to waveguide tee A23. Within waveguide scanner A1, waveguide tee A23 compares its inputs to produce an A minus C minus B minus D signal, which is absorbed by waveguide termination A30. More significantly, the tee produces an A minus C plus B minus D signal (Δ elevation signal) which is applied to azimuth/elevation scanner J334 (*b* below). At the same time, waveguide tee A22 compares its two inputs to produce an A plus C minus B plus D signal (Δ azimuth signal) to waveguide switch S13 (*c* below).

b. The azimuth/elevation scanner assembly consists of two hybrid tees separated by matched 180° ferrite phase shifter, each of which has two phase shift states; 0° or 180°. Phase status of the phase shifters is alternately reversed by 25-Hz ferrite scan pulses produced by scan generator A20. The Δ azimuth and Δ elevation signals are applied through the input hybrid tee of scanner J334 to the two 180°-ferrite phase shifters. The scan pulses alternately change the phase shifter states to apply the two error signals, in opposing phases, to the output hybrid tee. With inputs applied in this manner, the output hybrid tee alternately applies one composite error signal to directional coupler A31 while diverting the other signal to electrical load A32.

c. For automatic tracking of a satellite, waveguide switch S13 is positioned to apply the channel signal (solid lines) from waveguide tee A22 through the coupling section of directional coupler A31. Within the directional coupler, the channel signal mixes with the composite error signal and the composite error signal energy, not expended in the mixing process, is absorbed by electrical load A33. Waveguide switch S13 is controlled removely by means of the SUPPLEMENTAL CONTROL PENCIL BEAM pushbutton switch on the antenna control panel. For manual tracking of a satellite, waveguide switch S13 is remotely positioned to apply the channel signal directly to isolation filter FL2 (*d* below).

This signal (shown in dashed lines through switch S13) precludes 0.3 inherent loss through directional coupler A31. The direct-signal condition prevails when the PENCIL BEAM pushbutton switch is depressed.

d. Isolation filter assembly FL2 provides filtering action by means of 15 fixed-tuned cavities. It passes only the receive channel frequencies with a 7.25-GHz to 7.75-GHz band. Isolation provided by filter FL2 and rejection provided by bandpass filter FL8 (para 2-15*f*) minimize transmitter noise in the receive circuits. Waveguide assembly A34 applies the filtered receive signal to directional coupler A35.

e. Directional coupler A35 provides injection ports for close-loop testing of the receive function of the parametric amplifier. The main signal path through directional coupler A35 normally passes the receive sum signal to a parametric amplifier. One test input port is permanently connected as an injection port for a test translator signal and the opposite test port is normally terminated with a waveguide termination that is removed to provide an injection point for an external test signal during alignment and calibration procedures. The test translator function is described in paragraph 2-55.

2-52. Receive Signal Amplification Circuits

(fig. FO 2-2, sheet 4)

a. Receive signal amplification is accomplished in two stages. The first stage utilizes a three-stage parametric amplifier which is a low noise amplifier (LNA). The second stage utilizes an interconnect facility link amplifier (IFLA) which consists of a low noise traveling wave tube (TWT). Each stage has a gain of approximately 30 db. The receive signal amplification circuits are totally redundant from the input port of the LNA to the output port of the TWT and can be operated in any one of four loop configurations. Loop configurations are set up by selecting the desired LNA/TWT combination using switching circuits located on test translator panel 1A2A26 in the electronics shelter. In the normal receive mode of operation (with the test translator inhibited), the console operator can select signal paths through the amplification circuits to the frequency downconverter as follows:

(1) LNA1, isolator 1, and TWT 1.
(2) LNA2, isolator 2, and TWT 2.
(3) LNA1, isolator 2, and TWT 2.
(4) LNA2, isolator 1, and TWT 1.

b. Provision for monitoring the off-line signal path during normal operation is made available through the DOWNCONVERTER-DETECT switch, and GAIN MONITOR meter, in conjunction with the Test Translator, all located on the test translator control panel.

c. The three stages of rf amplification provided by the AM-6676/TSC-54 are functionally the same. Some differences occur in parameter values and physical layout but do not affect the final result. Overall, the parametric amplifier provides a 30 db gain for receive signals in a 7.25-to 7.75-GHz range with an instantaneous 1-db bandwidth greater than 500 MHz. There is 10-db amplification per stage with a 600-MHz stage bandwidth. An interstage bandpass filter (FL2) determines the system bandwidth of 500 MHz.

(1) The incoming microwave signal is applied from the input waveguide to the input port of circulator HY1. The signal entering the input port of the circulator is attenuated for a power loss of approximately 0.6 db as it flows to paramp AR1. The power level of the rf signal in the opposite direction (toward the input port of the circulator from the paramp) is attenuated approximately 40 db. (The power level is either aided or impeded by a strong magnetic field.) The incoming micro-wave signal is amplified by 10 db in paramp AR1 and the amplified signal is present at the same AR1 port. The amplified signal now flows back through circulator HY1 to its output port with a power loss of approximately 0.3 db. Circulator HY1 separates the input and output signals, provides low vswr and good impedance matching, and isolates paramp AR1 from the input and output signals.

(2) Within paramp AR1, interaction of low input signal power, in the range from 7.25 to 7.75 GHz, and a high pump power signal at 42 GHz, in a varactor diode, increases the input signal to a much higher level. The varactor mounted in a suitable structure comprises the paramp. Generally, the physical dimensions and arrangement of paramp AR1 provide three tuned circuits: the input signal frequency (7.25 to 7.75 GHz), the pump frequency (42.0 GHz), and the idler frequency (34.2 to 34.8 GHz). Careful components arrangement and pump filter FL1 prevents propagation of the idler signal through the circulator or the pump circuits. Amplifier gain is controlled primarily by controlling the level of pump power (generated by the Gunn oscillator) at the varactor diode. The center operating frequency and instantaneous bandwidth are controlled primarily by the amplitude of the bias voltage (0 to 6 volts) on the diode.

(3) A gunn-effect diode oscillator is used as

the pump source. The first-stage Gunn oscillator (A6Y1) produces a minimum power output of 95 mW. The second-and third-stage oscillators (A7Y1 and A8Y1, respectively) produce a minimum power output of 75 mW each. The oscillators are tunable over a range from 41.95 to 42.05 GHz. However, they are set for 42.0 GHz for Parametric Amplifier AM-6676/TSC-54.

(4) Isolators A6AT1, A7AT1, and A8AT1 are used with each Gunn oscillator to provide a constant load to isolate the oscillators from other circuits. Each isolator has an insertion loss of 0.2 db or less and provides isolation of 15 db or more at 42.0 GHz. Input vswr is 1.15 or less at 42.0 GHz.

(5) Pump power for each stage is sampled by 18-db crossguide couplers A9DC1, A10DC2, and A11DC1. The insertion loss of the coupler is 0.2 db. The sampled pump power for each stage is rectified by crystal detectors A9CR1, A10CR1, and A11CR1. The output of each detector produces a test point voltage of approximately 0.5 vdc.

(6) The gain, and to some extent the bandwidth, of the amplifier stages are affected by the pump power level at the varactor diode. To adjust the power level in each stage, a variable waveguide attenuator (A9AT1, A10AT1, A11AT1) is used. A lossy card (100 ohms per square inch) is inserted into the pump waveguide by a screw adjustment. The positioning of the card is set during gain-bandwidth alignment procedures. Attenuation is variable from 0 db to more than 20 db. Insertion loss is about 0.1 db. Attenuation variation is not directly translated into gain variation.

(7) To prevent sum and difference frequencies (49.50 GHz and 34.50 GHz) from feeding back into the pump circuit, a passband waveguide filter (A9FL1, A10FL1, A11FL1) is used at the paramp pump port. The filter provides at least 15 db attenuation at the sum difference frequencies and has an insertion loss of 0.2 db at 42.0 GHz. A step twist (A9W1, A10W1, A11W1) located between the pump filter and variable attenuator, provides addition filtering.

(8) A bandpass filter (FL2) is used to interconnect the first and second amplifier stages.
Insertion loss within the signal band (7.5 $\pm$ 0.25 GHz) is about 0.2 db. From 7.90 to 8.40 GHz the filter provides more than 20 db attenuation.
This filter is symmetrical, having equal attenuation (20 db) at frequencies less than 7.10 GHz, and therefore determines the passband of the amplifier.

(9) The bias voltage from voltage regulator PS1A3 is routed through three one-kilohm potentiometers (R1, R2, R3) connected in parallel. Each potentiometer pick-off provides the varactor bias voltage for one stage of the amplifier. The pick-off voltage is adjustable from 0 to +6 vdc and is set for each amplifier stage during gain-bandwidth alignment. The bias voltage on the varactor diode is the principal bandwidth and center frequency control of the amplifier.

(10) The bias voltage to each paramp is routed through a two-pole switch (S1, S2, S3). The other pole of the switch is connected directly to the +6.0 vdc terminal of the potentiometer (R1, R2, R3). When the switch is in the ON position the bias voltage from the pick-off arm of the potentiometer is applied to the varactor diode. When the switch is set to the BYPASS position, +6 vdc is applied to the varactor diode. The 6-volt bias moves the operating frequency of varactor diode out of the passband of the amplifier and effectively turns off the amplification stage but permits otherwise normal operation.

2-53. Frequency Downconversion
(fig. FO 2-2)

a. The amplified receive signal output from the IFLA amplifier is applied to power divider HY-1 (sheet 7) a passive waveguide device. The directional coupler splits the associated composite input into three equal-level signals for application to each downconverter.

b. The 7.25-to 7.75-GHz rf signal from the signal divider is applied to the downconverter through rf input stripline assembly DC1. This assembly isolates filters FL1 and FL2 from standing waves introduced by the signal divider assembly. Also, the assembly provides facilities for inserting an rf test signal into the downconverter through connector J2. Termination AT1 provides the 50-ohm terminating impedance required by connector J2 when a test signal is not used. The use of filter FL1 or FL2 is determined by the frequency of the input signal. The filters provides 3-db bandwidths of 7.25 to 7.55 GHz and 7.50 to 7.75 GHz, respectively.

c. The output of filter FL1 and FL2 is applied to the conversion stripline assembly where it is mixed with the 6.55-to 7.05-GHz local oscillator signal from the rf phase-locked oscillator unit. The resulting 700-MHz if. signal is applied to the 700-MHz if circuit for amplification and filtering. The 700-MHz if. circuit consists of amplifier AR1 and filter FL3. Amplifier AR1 amplifies the 700-MHz if. signal from the rf conversion stripline assembly by a factor of 20 db. Filter FL3,

which follows, restricts the if. bandwidth to between 680 and 720 MHz.

d. The rf conversion assembly also provides a 6.55-to 7.05-GHz local oscillator test output and a dc voltage that is proportional to the local oscillator input power level. The test output is routed to front panel RF LO SAMPLE connector J3. The dc voltage is applied to STATUS meter M1 through status indicator calibration unit A3 and STATUS SELECTOR switch S1. Termination AT2 provides the 50-ohm terminating impedance required by connector J3 when the test output is not used.

e. The local oscillator signal is generated by a 1.31-to 1.41-GHz microwave signal source and an X5 frequency multiplier in rf phase-locked oscillator unit Y1 (sheet 6). The signal source is phase locked to the 131-to 141-MHz signal from the frequency synthesizer (sheet 5) to provide precise control and stability. An indication of phase lock is provided by the oscillator phase lock output. If the signal source drops out of phase lock, the voltage appearing at this output activates out-of-lock detector unit A4. This action causes RF LO lamp DS2 to illuminate, activates audible alarm DS4, and provides a relay contact closure for a remote alarm circuit. A sample of the frequency control voltage used to maintain the signal source in phase lock is provided at the rf local oscillator. The frequency control voltage sample is applied to meter M1 through status indicator calibration unit A3 and switch S1.

f. The 700-MHz if. signal (sheet 7) from filter FL3 (c above) is applied to the if conversion stripline assembly where the signal is mixed with the 630-MHz local oscillator signal from if phase-locked oscillator Y2. The resulting 70-MHz if. signal is applied to the if output circuit for amplification and equalization. The if conversion stripline assembly also provides a 630-MHz local oscillator test output and a dc voltage which is proportional to the local oscillator input power level. The test output is routed to front panel IF LO SAMPLE connector J5. The dc voltage is applied to meter M1 through status indicator calibration unit A3 and switch S1. Termination AT3 provides the 50-ohm terminating impedance required by connector J5 when the test output is not used.

g. The 630-MHz local oscillator signal is generated by a voltage tuned oscillator in the if phase-locked oscillator unit (sheet 6). The oscillator operates in a phase-locked loop which is controlled by the 10-MHz signal from the frequency synthesizer (sheet 5). The 10-MHz signal is applied to the if phase-locked oscillator unit through power monitor CR3 to provide signal level monitoring (sheet 6). The dc voltage developed by the power monitor, which is proportional to the 10-MHz signal level, is applied to meter M1 through indicator calibration unit A3 and switch S1. An if local oscillator tuning output is also produced by the if phase-locked oscillator unit. This dc output, which represents the oscillator frequency control voltage, is applied to out-of-lock detector unit A4 and to meter M1 through status indicator calibration unit A3 and switch S1. When the oscillator is out of phaselock, an ac voltage is impressed on the if local oscillator tuning output. This voltage activates unit A4. The activation of unit A4 causes IF LO lamp DS3 to illuminate, activates audible alarm DS4, and provides a relay contact closure for a remote alarm circuit.

h. The 70-MHz if signal (*f* above) is applied to amplifier AR2 (sheet 7), which provides a gain of approximately 32 db. Amplifier AR2 is followed by phase equalizer EQ1, which compensates for phase nonlinearities generated in the downconverter if circuits, and amplitude step attenuator AT5, which adjusts overall downconverter gain. Amplifier AR3, which follows the equalizer and attenuator, provides an additional gain of 32 db to compensate for the losses incurred during equalization. The output of amplifier AR3 is applied to output connector J6 through directional coupler DC2. Directional coupler DC2 provides a 70-MHz if test output, which is applied to front panel 70 MHz SAMPLE connector J7. Termination AT4 provides the 50-ohm terminating impedance required by connector J7 when not in use.

i. The 70-MHz outputs from each downconverter is applied to the communications patching panel for routing to the AN/TSC-54 comm/ beacon demod assemblies, the URC-61 and TCC-79.

2-54. Communication Signal Patching

a. The if patch panel functions as an interconnecting point for all signals to and from the AN/TSC-54 transmitting and receiving equipment. Transmit signals from the 1A3A14 modulator, the AN/URC-61 and the AN/TCC-79 (when used with the AN/TSC-54) are made available at the if. patch panel for application to the upconverters. For example, a 70-MHz communications signal patched from coupler CP3 to coupler CP8 is patched from TCC-79 jack to UP CONV. 1 jack.

b. Communications signals, extracted from the receive signal by the downconverters, are made available at the if. patch panel for application to the

AN/TSC-54 comm and beacon demods, the AN/URC-61, and the AN/TCC-79. For example, a 70-MHz communications signal applied from coupler CP12 to coupler CP20 is patched from DOWN CONV. 1 jack to COMM. DEMOD 1 jack. Both transmit and receive signals available to any other signal jack to provide versatility of systems configuration.

c. The FM demodulator of the AN/TCC-79 provides an OBN signal to the OBN monitor panel via external signal distribution panel 1A10 for monitoring the quality of the received signal.

2-55. Receive Circuits Loop Testing Circuits
(fig. FO 2-2)

Test translator circuits incorporated in Satellite Communication Terminal AN/TSC-54 provide a capability for loop testing the receive function circuits. The test translator combines a transmit signal sample with a test translator developed Io frequency to produce an if. signal having a frequency within the receive band. The simulated receive signal can be selectively injected at various test ports along the receive signal processing path and then processed like the normally received satellite signal in order to test the receive circuits.

a. Rf oscillator A4 (sheet 1) is activated when +28 vdc is applied to oscillator power jack J2 via test translator oscillator control relay K1. Control relay K1 is energized when INJECTION SIGNAL-ON/OFF switch/indicator A4 on test translator control panel 1A2A26 is in the ON position (fig. FO 2-5, sheet 2) Activated in this manner, oscillator A4 generates a fixed frequency cw signal; a crystal oven within the oscillator ensures frequency stability. A limited-range adjustment control on the oscillator allows compensation for minor frequency drifts incurred by crystal aging. Cable W6 routes the cw signal to power divider A13.

b. Power divider A13 receives the cw signal at input jack J1 and applies most of the signal through output jack J2 and coaxial cable W7 to harmonic generator A12. A cw sample signal, 15 db lower than the input, is branched to output jack J9 of bulkhead adapter CP4. From output jack J9, the cw signal is applied to the J13 end of the bulkhead adapter CP1. At the opposite end of bulkhead adapter CP1, coaxial termination AT1 absorbs the cw signal sample, except when removed for equipment tests.

c. The basic cw signal, with its harmonics, is applied to harmonic generator A12 through input connector P1. An inductor-capacitor parallel tank circuit within harmonic generator A12 is fixed-tuned to resonate at the sixth harmonic of the applied signal. Thus, the sixth harmonic frequency is perpetuated along the signal flow while the basic cw signal and other harmonics are rejected.

d. The bandpass filter receives the extracted sixth harmonic frequency (test translator local oscillator signal) by mating of its input connector P1 with output jack J1 of harmonic generator A12 (*c* above). The local oscillator signal, at the center of the filter's response curve, is passed unimpeded while sporadic signals and harmonics more than 7.2 MHz on either side of center are attenuated 3 db, and signals more than 118 MHz on either side of center are attenuated 50 db. Tandem coaxial cables W30, W31, and W29 route the filtered LO signal to fixed attenuator AT6.

e. Power of the local oscillator signal is reduced 16 db as it passes through fixed attenuator AT6. Coaxial cable W33 applies the reduced level signal to a variable attenuators, each stradled by two coaxial switches. Attenuator and switch interconnection is such that any or all switch pairs can be remotely actuated to insert or remove their associated fixed attenuators. This feature allows manually controlled variations of the local oscillator signal level. Since the power level of the final test signal varies linearly as the local oscillator signal varies, the test signal can be adjusted in 31-db steps over a 31-db range for loop testing under simulated weak, intermediate, and optimum signal conditions.

(1) Except for attenuation capabilities, the five switchable segments of the variable attenuation network are alike and perform similarly. Fixed attenuators AT1 through AT5 differ in that they provide 1, 2, 4, 8, and 16 db attenuation, respectively. Identical input and output coaxial switches comprise a switch pair for each fixed attenuator. Each coaxial switch has two mechanically linked, single throw, electromagnetically actuated contacts. When one contact is connected to the associated fixed attenuator, the opposite contact is connected to ground, and vice-versa.

(2) Both switches of a switch pair are simultaneously energized or deenergized by manually selected control voltages from a set of five ATTENUATION toggle switches on the control panel (fig. FO 2-5, sheet 2). Since all switchable segments of the attenuation network are similarly controlled, only the 1-db control is discussed.

(3) When set to the 1-db position, ATTENUATION toggle switch S3 applies +28 vdc unregulated through filter FL12B1 and filter FL2C3 in the elevation cable wrap assembly, to pin 4 of coaxial

switches S1 and S2. Both switches energize simultaneously and disconnect attenuator bypass cable W5 and insert 1-db fixed attenuator AT1 in the local oscillator signal path.

(4) Conversely, when returned to the off (down) position, TEST TRANSLATOR OUTPUT toggle switch S3 disconnects the +28 vdc ((3) above) allowing coaxial switches S1 and S2 to deenergize to positions shown. In the deenergized state, the coaxial switches disconnect 1-db fixed attenuator AT1 and insert attenuator bypass cable W5 in the local oscillator signal path. In this manner, any combination of 1, 2, 4, 8, and/or 16 db of attenuation in 1-db steps. The level-controlled output signal at jack J2 of coaxial switch S12 (sheet 2) is applied to waveguide crystal mixer A9.

f. Waveguide crystal mixer A9 combines the level-controlled local oscillator signal injected at input jack J3 with a transmit test signal applied through its input waveguide port. The transmit test signal is a sampling derived at directional coupler W7 (fig. FO 2-1, sheet 14) and enters the test translator through remotely controlled waveguide switch S6. This switch terminates the transmit input when the translator is off (INJECTION SIGNAL switch/indicator on the control panel to OFF). The control of waveguide switch S6 is shown on (fig. FO 2-5, sheet 2). Mixing of the local oscillator and transmit test signals produce an if. signal having a frequency within the receive band. Two output jacks on waveguide crystal mixer A9 (sheet 2) are metering circuit connections. The forward and reverse crystal currents output at mixer jacks. J1 and J2 respectively, can be selectively monitored on the control panel MIXER CURRENT meter by setting the associated selector switch to the appropriate position (FWD or RVS). A short waveguide adapter routes the test translator signal from a waveguide flange on waveguide crystal mixer A9 to rf reflection isolator AT11.

g. Pneumatic control bleed valve A36 is installed externally in a threaded hole in the short waveguide adapter (*f* above). The bleed valve has a 0.18-inch diameter exhaust orifice that can be manually opened for waveguide purging during routine maintenance of the equipment.

h. Rf reflection isolator AT11 allows unimpeded forward passage of the test translator signal while attenuating reflected signals 20 db across the 7.25 to 7.75-GHx receive band. Since the rf reflection isolator is symmetrically shaped, it is prominently marked with signal-IN and signal-OUT directions to preclude reversal during assembly after repairs.

i. The output of rf reflection isolator AT11 is applied through variable attenuator AT10 and waveguide-to-coaxial adapter CP3 to coaxial switch S14. Variable attenuator AT10 is used to preset the level of the test translator circuits. Variable attenuator AT10 is manually set and locked during test translator alignment. The calibrated attenuation value of the injected test translator signal closely parallels a normal receive signal applied to ;he frequency translator circuits.

j. The operation of coaxial switch S14 is controlled by control panel INJECTION POINT switch S2 as depicted on (fig. FO 2-5, sheet 2). The INJECTION POINT switch determines the point along the signal path that the test translator signal is inserted.

(1) When switch position one is selected, +28 vdc unregulated is routed to pin A of S14. This electrically connects the common input of S14 to pin (sheet 2) thus applying the test translator signal to the antenna probe path. Power divider A14 receives the test translator signal at input jack J1 and develops equal-level output signals at jacks J2 and J3. Coaxial cables W1 and W2 separately apply the test translator signal to waveguide-to-coaxial adapters CP1 and CP2, respectively. The adapters are attached by waveguide flanges to open-ended waveguide assemblies A15 and A16, mounted at the center and just inboard of the left and right of fold joints on the antenna reflector, emit the test translator signal to spray the subreflectors of the four DIELGUIDES with equal intensity. After entering the DIELGUIDES the test translator signal follows the normal receive signal processing path to the demodulators.

(2) With the control panel INJECTION POINT switch set to position 2, +28 vdc unregulated is routed to pin B of S14, connecting the common input to pin 2. This inserts the test translator signal between the antenna and the on-line parametric amplifier. The signal path in this position is from pin 2 of S14 (sheet 2) through coaxial cable W34 to waveguide-to-coaxial adapter CP2 (sheet 3) and variable attenuator AT7. Variable attenuator AT7 is used for manually presetting the test translator signal to ensure a calibrated-level signal output for the parametric amplifier. During test translator calibration, variable attenuator AT7 is set and locked to provide 30 db attenuation corresponding with the test signal gain achieved through the parametric amplifier. A variable attenuator is necessary so that the

gain differences of the parametric amplifiers used in the AN/TSC-54 can be compensated for by attenuation value changes of variable attenuator AT7. The test translator signal is routed to the test port of directional coupler DC1 through waveguide-flange connections. After entering directional coupler DC1, the test translator signal is routed along the normal receive signal processing path.

(3) With the control panel INJECTION POINT switch set to position 3, +28 vdc unregulated is routed to pin C of S14, connecting the common input to pin 3. This inserts the test translator signal at the input of the off-line parametric amplifier. The signal path in this position is from pin 3 of S14 (sheet 2) through coaxial cable W35 to waveguide-to-coaxial adapter CP1 (sheet 4) and pin 2 of waveguide switch S7. Pin 2 of S7 is always connected to the off-line parametric amplifier. The operation of S7 is controlled from control panel switch/indicator A1, as depicted on figure FO 2-5, sheet 3.

(4) With the control panel INJECTION POINT switch set to position 4, +28 vdc unregulated is routed to pin D of S14, connecting the common input to pin 4. This inserts the test translator signal at the input of TWT 1. The signal path in this position is from pin 4 of S14 (sheet 2) through coaxial cable W36 to 10-db directional coupler DC2 (sheet 4), to TWT 1. The path from TWT 1 is determined by the position of waveguide switch S15 which is controlled from control panel switch/indicator A3, as depicted on figure FO 2-5, sheet 3.

(5) With the control panel INJECTION POINT switch set to position 5, +28 vdc unregulated is routed to pin E of S14, connecting the common to pin 5. This inserts the test translator signal at the input of TWT 2. The signal path in this position is from pin 5 of S14 (sheet 2) through coaxial cable W38 to 10-db attenuator DC3 (sheet 4), to TWT 2. The path from TWT 2 is determined by the position of waveguide switch S15, which is controlled from control panel switch/indicator A3, as depicted on figure FO 2-5, sheet 3.

k. The test translator control panel (fig. FO 2-5, sheet 3) also controls which combination of parametric amplifier (LNA 1 or LNA 2) and TWT (TWT 1 or TWT 2) will be on-line. Two-segment, black-lighted switch/indicators A1, A2, and A3 control the status of waveguide switches S7, S16, and S15, respectively (sheet 4). In addition to selecting the on-line components, the switch/indicators connect the off-line parametric amplifier and TWT into the GAIN MONITOR circuit so that the off-line components may be checked by injecting the test translator signal to the off-line components and monitoring the GAIN MONITOR meter on the control panel. Since there are four possible combinations of off-line components, each combination has an individual meter calibration resistor. All three switch/indicators (fig. FO 2-5, sheet 3) are identical. The top set of contacts apply control voltage to the appropriate waveguide switch. A return path through the waveguide switch causes one of the segment lamps to light indicating the switch position selected. The off-line output (pin 4) of waveguide switch S15 (sheet 4) is detected by detector/amplifier A7 and routed from P10-E of A7 (fig. FO 2-5, sheet 3) to the lower set of contacts of switch/indicator A1. The lower set of contacts route the detected test translator signal to the appropriate meter calibration resistor to the meter. The TEST TRANSLATOR/PILOT GENERATOR switch on the control panel is not used at this time.

l. An additional test translator is provided in the frequency conversion subsystem (1A19 console) for loop testing of the frequency conversion subsystem (fig. FO 2-5, sheet 4).

(1) The 7.9-to 8.4-GHz transmit signal from the upconverter is applied to the test translator conversion stripline assembly through RF INPUT connector J1. In the conversion stripline assembly, the transmit signal is mixed with a 200-or 725-MHz signal to provide a downconverted 7.25-to 7.75-GHz receive frequency signal. Selection of the local oscillator frequency is determined by the setting of 725 MHz-200 MHz toggle switch S4, which in turn, controls the operation of coaxial switches S2 and S3. Coaxial switch S2 connects the multiplier or phase-locked oscillator output to the conversion stripline assembly, while switch S3 applied the cesium beam frequency standard 5-MHz signal to either the multiplier or phase-locked oscillator input. Indicator lamps DS2 and DS3 illuminate to indicate the particular local oscillator circuit in use.

(2) The output signal is applied to RF OUTPUT connector J2 through LEVEL SET attenuator AT1 and isolator HY1. Attenuator AT1 is adjusted to simulate the desired satellite path loss. Isolator HY1 isolates the signal output of attenuator AT1 from mismatches which might be created by external load equipment. For monitoring purposes, a dc voltage proportional to the levels of the significant signals within the test translator are applied through status indicator calibration unit A1 and STATUS SELECT switch S1 to STATUS meter M1.

2-56. Parametric Amplifier Control Circuits

The parametric amplifier control panel, located within the parametric amplifier, contains the test points and controls necessary for gain and bandwidth alignment. Each amplification stage can be bypassed by activating the appropriate BYPASS SW S1, S2, or S3. For a detailed analysis of the control circuits, reference TM 11-5820-819-34.

2-57. Communications Demodulation

(fig. FO 2-2)

a. The frequency modulated 70-MHz carrier input signal at connector J1 of comm demod A3 (sheet 8) is applied through 70-MHz bandpass filter A1 to 70-MHz balanced mixer A2. The 70-MHz bandpass filter has a bandwidth of 4 MHz centered at 70 MHz and the signal is attenuated 5 db by bandpass filter A1. In addition to the 70 MHz signal, the 70-MHz/21.4-MHz balanced mixer receives a 1-millivolt 48.6-MHz signal, from the 48.6-MHz voltage-controlled oscillator (vco) A3. The two frequencies are mixed and the difference frequency of 21.4 MHz is applied to 21.4 MHz if. preamplifier A4. The 21.4-MHz signal is amplified and applied to input bandwidth select switch A5. The gain of the 21.4-MHz if. preamplifier is controlled by an automatic gain control (age) voltage from age amplifier A22 (*j* below). The 21.4-MHz if. preamplifier is capable of a gain of 50 db but the gain is controlled over a 40-db range by the age voltage. Input bandwidth select switch A5 contains five diode switches which are controlled by RECEIVE MODE switch S2 and matrix module A45 (*v* below).

b. The selected diode switch controls the application of the 21.4-MHz signal to the associated filter; 75-kHz bandpass filter A6, 150kHz bandpass filter A7, 300-kHz bandpass filter A8, 560-kHz bandpass filter A9, or 1000-kHz bandpass filter A10. The filters have a bandwidth of 75 kHz, 150 kHz, 300 kHz, 560 kHz and 1000 kHz respectively, centered at 21.4 MHz. Filters A6 and A7 are crystal filters and filters A8, A9 and A10 are IC filters. The 21.4MHz output of the selected filter is applied to the associated diode switch in output bandwidth select switch A11. The diode switch in output bandwidth select switch A11 is selected simultaneously with the associated diode switch in input bandwidth select switch A5.

c. The output of each of the five diode switches in the output bandwidth select switch is applied to 21.4 MHz post amplifier A12. The 21.4-MHz post amplifier amplifies the if. signal and provides six 21.4-MHz if. reference outputs and a detected envelope output. The detected envelope output is applied to relay module A48 at pin 9 of connector J1 (sheet 9). Five 21.4-If. reference outputs are applied to 21.4-MHz wideband discriminator A24 (sheet 8), 21.4-MHz narrowband discriminator A25, 21.4-MHz loop phase detector A16, 21.4/1.4-MHz balanced mixer A30, and 21.4-MHz am. phase detector A13, respectively (sheet 9). The sixth 21.4-MHz if. reference output is not used.

d. The 21.4 MHz wideband discriminator A24 sheet 8) is a wideband LC discriminator with a peak-to-peak bandwidth of 2 MHz. If the incoming 21.4-MHz if. carrier frequency changes, a dc voltage proportional to the frequency change is produced. The output of wideband discriminator-24 is applied to normally-open contact 3 of relay K1 in AFC and sweep module A29 (*r* below). 21.4-MHz narrowband discriminator A25 sheet 9) is a narrowband crystal discriminator with a peak-to-peak bandwidth of 200 kHz. If the incoming 21.4-MHz if. carrier frequency changes, a dc voltage that is proportional to the frequency change is produced. The output of narrowband discriminator A25 is applied to normally-closed contact 2 of relay K1 in AFC and sweep module A29.

e. The 21.4-MHz loop phase detector A16 sheet 9) is part of a phase lock loop circuit which s comprised of 21.4/1.4 MHz loop amplifier A21, 0-kHz loop filter A19, 30 kHz loop filter A18, 300 kHz loop filter A49, 1500 kHz loop filter A20, 1.4-MHz voltage-controlled oscillator (VCO) A17, and three-way power divider A15. The 21.4 MHz loop phase detector A16 receives the 1.4-MHz if. signal from 21.4-MHz post amplifier 112 and the 21.4 MHz phase 90° signal which is generated by the 21.4-MHz vco A17. The 90° phase shift is obtained by applying the 21.4-MHz vco signal from three-way power divider A15 through a cable which is electrically a quarter wavelength at 21.4 MHz. Provided the two 1.4-MHz signals remain at 21.4 MHz, the output of 21.4-MHz loop phase detector A16 is zero. If the 21.4-MHz phase 90° signal changes frequency, a dc voltage proportional to the phase difference between the two signals is produced at the output of 21.4-MHz loop phase detector A16.

f. The polarity of the dc error (*e* above) is dependent upon the direction of phase error. The dc error voltage is applied through the selected loop filter, A18, A19, A20, or A49 to the input of servo operational amplifier AR1 in 21.4/1.4-MHz loop amplifier A21. Without a dc error input, servo operational amplifier AR1 is biased at a dc level which produces a +7.9 vdc level

at the output. The +7.9 vdc level is applied to the 21.4MHz vco A17 which sets the output to 21.4 MHz. When the dc error signal is combined with the bias voltage at the input to servo operational amplifier AR1, the output dc level of AR1 is changed and produces a corresponding change in the 21.4-MHz vco A17 output frequency. This frequency is changed (increased or decreased) in the direction necessary to correct the phase error at the output of 21.4-MHz loop phase detector A16. In this manner, the output from the 21.4-MHz vco A17 is phase-locked to the incoming 21.4-MHz if. signal.

g. The modulating intelligence contained in the 21.4-MHz if. signal is detected by 21.4-MHz loop phase detector A16 and the resulting demodulated audio signal is applied to the normally open contact of relay K4 in relay module A48 and through the relay selected loop filter to the input of servo operational amplifier AR1 in 21.4-MHz loop amplifier A21. The selection of 50-kHz loop filter A19, 30-kHz loop filter A18, 300-kHz loop filter A49, or 1500-kHz loop filter A20 is performed by relays K1 through K3 in 21.4-MHz loop amplifier A21. Relays K1 through K3 are controlled by RECEIVE MODE switch S2 (sheet 5) and matrix module A45 (*v* below). The demodulated audio signal is amplified by servo operational amplifier AR1 and a portion of the output is applied as feedback through the selected loop filter to the input of AR1. The selected loop filter determines the bandwidth of the phase lock loop. The amplified demodulated audio signal is centered on the dc level which controls the 21.4-MHz frequency. The output of servo operational amplifier AR1 is applied to the 21.4-MHz vco A17 and to the normally closed contact of relay K4 in relay module A48.

h. The 0 dbm 21.4-MHz output of the 21.4 MHz vco A17 is applied to three-way power divider A15. The output of connector J1 of three-way power divider A15 is terminated by 50-ohm coaxial termination AT3. The output at connector J2 of three-way power divider A15 is applied through 90° phase shift cable A14 to 21.4-MHz loop phase detector A16. The output at connector J4 of three-way power divider A15 is applied to 21.4-MHz am. phase detector A13 which also receives the 21.4-MHz if. signal from 21.4-MHz post amplifier A12 (sheet 8). When the two 21.4-MHz signals are in phase, the 2.1.4-MHz phase lock loop is phase locked and 21.4-MHz am. phase detector A13 produces a coherent dc output of approximately +1 vdc. The coherent dc voltage, which represents the demodulated envelope, is applied through the normally closed contacts of relay K2 in relay module A48 to connector J1-6 of am. amplifier A44 (sheet 10) and to connector J1-8 of phase lock and sweep stop module A27. The demodulated envelope signal is amplified by am. amplifier A44 and the output is applied to the antenna control circuits.

i. The demodulated envelope signal at pin 8 of connector J1 of phase lock and sweet stop A27 is applied to an integrator operational amplifier AR1 which functions as a level detector. The reference level for the operational amplifier is +0.5 vdc. When the demodulated envelope input exceeds the reference level of +0.5 vdc, the output of the integrator operational amplifier is clamped at a maximum negative voltage. This negative voltage energizes the phase lock detect relay and +28 vdc is applied through the closed contacts to illuminate LOCK indicator lamp DS6. The other set of relay contacts applies a phase lock indication to the antenna control circuits. The negative output level of the integrator operational amplifier AR1 is applied as one input to an OR gate. The output of the OR gate biases an amplifier which energizes the sweep stop relay K3. When the sweep stop relay is energized, a ground is applied to afc and sweep module A29 (sheet 8) to prevent the afc and sweep from generating a sweep voltage. A long time constant (approximately 2 seconds) of the integrator operational amplifier AR1 in phase lock and sweet stop module A27 (sheet 10) prevents the sweep stop relay from deenergizing when the phase lock loop momentarily loses lock due to a very low input signal level.

j. The detected envelope signal from 21.4MHz post amplifier A12 (sheet 8) is applied through the normally closed contacts of relay K1 in relay module A48 (sheet 9) to connector J1-6 of the signal detect module A23 (sheet 10), connector J1-6 of agc amplifier A22, and connector J1-9 of am. amplifier A44. The detected envelope signal applied to am. amplifier A44 is amplified and applied to the antenna control circuits as a tracking error signal. The detected envelope signal applied to servo operational amplifier AR1 in agc amplifier A22 is amplified and applied to servo operational amplifier AR2.

The output of servo operational amplifier AR2 is applied as an agc voltage to 21.4-MHz if. preamplifier A4. The other outputs of servo operational amplifier AR1 in agc amplifier A22 are applied to SIGNAL STRENGTH meter M3, and to the antenna control circuits.

k. The detected envelope input to signal detect module A23 (*j* above) is applied to a filter which removes the dc component and the high frequency noise. The output of the filter is applied to a level detector which

triggers a 4-second monostable multivibrator when the input signal exceeds a certain level. The 4-second output pulse from the monostable multivibrator energizes relay K2. The 4-second pulse is also applied to the OR gate in phase lock and sweep stop module A27. When relay K2 energizes, a signal detect indication is applied from the closed relay contacts to the antenna control circuits. The 4-second pulse input to the OR gate causes the level detector operational amplifier to energize the sweep stop relay and inhibit the afc sweep. If the afc circuit has locked and brought the received signal into the center of the if. passband, the phase lock loop will lock and the demodulated envelope input to the integrator operational amplifier level detector at pin 8 of connector J1 becomes sufficient to cause the level detector output to be clamped at a maximum negative level. The negative level is applied to the OR gate and assumes control of the sweep stop relay, keeping the relay energized.

l. The communication demodulator also generates a second 1.4-MHz if. frequency. This is accomplished by mixing the 21.4-MHz if. signal from 21.4-MHz post amplifier A12 with the 20-MHz frequency from X4 frequency multiplier A28 (sheet 9). The X4 frequency multiplier receives the 5-MHz reference frequency from the 5-MHz distribution amplifier and multiplies it by a factor of 4 to produce a 20-MHz signal. The X4 frequency multiplier is enabled by relay K1 which is controlled by RECEIVE MODE switch S2 and the matrix module A45. Operation of the RECEIVE MODE switch and the matrix module is covered in *v* below. The 20-MHz output of X4 frequency multiplier A28 is applied to the 21.4/1.4-MHz balanced mixer A30 and 1.4-MHz discriminator A26. The 21.4-MHz if. signal and the 20-MHz signal are mixed and the resulting 1.4-MHz if. signal is applied to a resistor network composed of resistors R1, R2, and R3 in 1.4-MHz if. predetect switch A31. Relay K1 in the 1.4-MHz predetect switch is controlled by the RECEIVE MODE switch. When relay K1 is deenergized, the 1.4-MHz if. signal is applied through the normally closed contacts of relay K1, 10-kHz bandpass filter A33, normally closed contacts of relay K1 (also controlled by the RECEIVE MODE switch), resistors R1, R2, and R3 in 1.4-MHz if. select switch A46 to 1.4-MHz post amplifier A34. When both K1 relays are energized, the 1.4-MHz if. signal is applied through 4-kHz bandpass filter A32 to 1.4-MHz post amplifier A34. The 1.4-MHz post amplifier A34 amplifies the 1.4-MHz if. signal and provides four 1.4-MHz outputs and a detected envelope output. The detected envelope output is applied to the normally open contact of relay K1 in relay module A48. Relay K1 is controlled by the RECEIVE MODE switch, and when the relay is energized, the 1.4-MHz detected envelope signal is applied to the output of relay module A48 in place of the detected envelope signal from 21.4-MHz post amplifier A12 (*i* and *j* above). One of the 1.4-MHz outputs of 1.4-MHz post amplifier A34 is terminated by coaxial termination AT4. The other 1.4 MHz outputs are applied to 1.4MHz loop phase detector A36, 1.4 MHz discriminator A26, and 1.4-MHz loop phase detector A37, respectively.

m. The 1.4-MHz loop phase detector A36 (*l* above) is part of a phase lock loop circuit which is comprised of 1.4-MHz loop amplifier A40, 550-Hz loop filter A42, 275-Hz loop filter A41, 1.4-MHz VCXO A38, two-way power divider A39 (sheet 10) and 90ø difference phase shifter A35. The 1.4-MHz loop phase detector A36 (sheet 9) receives the 1.4-MHz if. signal from 1.4-MHz post amplifier A34 and a 1.4-MHz phase 90° difference phase shifter A35. The 1.4-MHz phase 90° signal is generated by 1.4-MHz VCXO A38 and then applied through two-way power divider A39 to 90° difference phase shifter A35. Provided the two 1.4-MHz signals are in phase, the output of 1.4-MHz loop phase detector A36 is zero. If the 1.4-MHz phase 90° signal changes frequency, a dc error voltage, proportional to the phase difference between the two signals, is produced at the output of 1.4-MHz loop phase detector A36. The polarity of the dc error voltage is dependent upon the direction of phase error. The dc error voltage is applied through the selected loop filter, 550 Hz loop filter A42 or 275-Hz loop filter A41, to the input of operational amplifier AR1 in 1.4-MHz loop amplifier module A40. Without a dc error input, operational amplifier AR1 is biased at a dc level which produces a +7.9-vdc level at the output. The +7.9 vdc is applied to 1.4-MHz VCXO A38 to set the output to 1.4 MHz. When the dc error signal is combined with the bias voltage at the input of operational amplifier AR1, the output level of AR1 is changed and produces a corresponding change in the 1.4-MHz output frequency in the direction necessary to correct the phase error at the output of 1.4-MHz loop phase detector A36. In this manner, the output from 1.4-MHz VCXO A38 is phase locked to the incoming 1.4-MHz if. signal.

n. The modulating intelligence contained in the 1.4-MHz if. signal, is detected by 1.4-MHz loop phase detector A36 and the resulting demodulated audio signal

is applied to the normally open contact of relay K4 in relay module A48 and through the relay selected loop filter to the input of operational amplifier AR1 in the 1.4-MHz loop amplifier A40. The selection of 550-Hz loop filter A42 or 275-Hz loop filter A41 is performed by relay K1 which is controlled by the position of RECEIVE MODE switch S2 and matrix module A45. The demodulated audio signal is amplified by operational amplifier AR1 and a portion of the output is applied as feedback through the selected loop filter to the input of amplifier AR1. The selected loop filter determines the bandwidth of the phase lock loop. The amplified demodulated audio signal is centered on the dc level which controls the 1.4-MHz frequency. The output of operational amplifier AR1 is applied to 1.4-MHz VCXO A38 and to the normally closed contact of relay K4 in relay module A48.

o. The o dbm/1.4-dbm 45° phase output of 1.4-MHz VCXO A38 is applied to three-way power divider A39 (sheet 10). One output of the power divider is terminated by coaxial termination AT5 and the other output is applied to 90° difference phase shifter A35. The 90° difference phase shifter provides two outputs which are 90° apart. The 1.4-MHz 45° phase input is inductively phase shifted +45° to provide a 1.4-MHz 0° phase output which is applied to 1.4-MHz am. phase detector A37. The 1.4-MHz 45° phase input is also capacitively phase shifted-45° to provide a 1.4-MHz 90° phase output which is applied to 1.4-MHz loop phase detector A36 (m above).

p. The 1.4-MHz am. phase detector A37 (sheet 10) receives the 1.4-MHz 0° phase signal from 90° phase difference phase shifter A35 and the 1.4-MHz if. signal from 1.4-MHz post amplifier A34 (sheet 9) and produces a coherent dc voltage of approximately +1 vdc when the 1.4-MHz phase lock loop is locked. When the phase lock loop is not locked, the two input signals are not in phase and 1.4-MHz am. phase selector A37 does not produce the coherent dc output. The coherent dc voltage, which represents the demodulated envelope, is applied to the normally open contact of relay K2 in relay module A48. When relay K2 is energized, the 1.4-MHz demodulated envelope is selected in place of the 21.4-MHz demodulated envelope as the output of the relay module. When selected, the 1.4-MHz demodulated envelope performs the same functions as the 21.4 MHz demodulated envelope. Relay K2 is also controlled by the position of RECEIVE MODE switch S2 and matrix module A45.

q. The 1.4-MHz discriminator A26 (sheet 8) has a peak-to-peak bandwidth of 15 kHz. It receives the 20-MHz reference input from X4 frequency multiplier A28 (sheet 9) and the 1.4-MHz if. signal from 1.4-MHz post amplifier A34. These two signals are mixed to produce the 21.4-MHz if. signal which is applied to the crystal discrimination in 1.4-MHz discriminator A26 (sheet 8). If the incoming 1.4-MHz if. frequency changes, the crystal discriminator produces a dc voltage proportional to the amount of frequency shift. This dc voltage is applied to the normally open contact of relay K2 in afc and sweep module A29.

r. Afc and sweep module A29 receives the outputs of 21.4-MHz wideband and narrowband discriminators A24 and A25, 1.4-MHz discriminator A26, and a sweep stop signal from phase lock detect and sweep stop module A27 (*k* above). When the afc loop is locked, the dc error output from the selected discriminator is applied through the contacts of relays K1 and K2 (or relay K2 only) to operational amplifier AR1. The dc error voltage is amplified by operational amplifier AR1, the sweep circuit, and by operational amplifier AR3. The output of operational amplifier AR3 is applied to the 48.6-MHz vco A3 to change the 48.6-MHz frequency, in a direction and by an amount necessary, to return the selected discriminator output to zero. At this time, the sweep circuit in afc and sweep module A29 is disabled by a ground applied at pin 1 of connector J3 from phase lock detect and sweep stop module A27.

s. If the afc loop unlocks and stays unlocked in excess of 2 seconds, the ground is removed from connector J3 (*r* above) and the sweep circuit starts producing a sawtooth sweep voltage that is amplified by operational amplifier AR3 and then applied to the 48.6-MHz vco A3. The sawtooth sweep is centered on the dc level which controls the 48.6-MHz frequency and causes it to vary above and below 48.6-MHz. When the received signal is again of sufficient strength, it produces an increase in the detected envelope input from 21.4-MHz post amplifier A12 to signal detect module A23 (sheet 10) and the afc loop will again be locked. Signal detect module A23 then applies a 4-second pulse to phase lock and sweep stop module A27, energizing the sweep stop relay which in turn applied a ground to pin 1 of connector J3 of afc and sweep module A29 (sheet 8). This ground inhibits the sweep circuit, and the output of the selected discriminator assumes control of the 48.6-MHz VCO A3. Assuming that the afc loop has locked and brought the received signal into the center of the if.

passband, the 21.4-MHz and 1.4-MHz if. phase lock loops lock almost instantaneously. When the phase lock loops lock, the selected demodulated envelope signal input at pin 8 of connector J1 of phase lock and sweep stop module A27 (sheet 10) causes the phase lock detect circuit to assume control of the sweep stop relay K3.

t. Demodulator 48.6-MHz VCO A3 (sheet 8) may be manually controlled by setting TUNING MODE switch S1 to MAN. This opens the sweep circuit control line which inhibits the sweep circuit. VCO MANUAL TUNING potentiometer R1 is connected to the input of operational amplifier AR3 and is adjusted to control the output level of the operational amplifier. This causes the frequency of the 48.6-MHz vco A3 to either increase or decrease, depending upon the direction that the potentiometer is turned. When TUNING MODE switch S1 is set to afc, the sweep circuit output is applied to VCO TUNING meter M1. VCO TUNING meter M1 is calibrated in kc and indicates the amount of frequency deviation that the sweep circuit output will produce in the 48.6-MHz vco A3. Relays K1 and K2 in afc and sweep module A29 are controlled by the position of RECEIVE MODE switch S2 and matrix module A45.

u. Relay K4 in relay module A48 (sheet 9) has two sets of contacts. One set of contacts receives the amplified demodulated audio signal of 21.4-MHz loop amplifier A21 at the normally-closed contact and the demodulated audio signal of 21.4-MHz loop phase detector A16 at the normally-open contact (*g* above). The other set of contacts receives the amplified demodulated audio signal of 21.4/1.4-MHz loop amplifier A40 at the normally-closed contact and the output of 1.4-MHz loop phase detector A36 at the normally open contact (n above). With relay K4 deenergized, the outputs of the loop amplifiers are applied through relay K4 to relay K3; when relay K4 is energized, the outputs of the loop phase detectors are applied through relay K4 to relay K3. Relay K3 controls the application of the demodulated audio signal applied to 0-30 db attenuator and audio amplifier A43 (sheet 10). Relays K3 and K4 are controlled by the position of RECEIVE MODE switch S2 and matrix module A45. The 0-30 db attenuator and radio amplifier A43 contains four attenuators of 2, 4, 8, and 16 db, respectively. These attenuators can be switched in any combination to provide the desired demodulated audio signal level input to the audio amplifier. The 0-dbm output of the audio amplifier is applied to BASEBAND LEVEL meter M2 and through an isolation transformer TI to the DEMODULATOR LINE jacks on the baseband patch panel (para 2-58).

v. RECEIVE MODE switch S2 (sheet 8) and matrix module A45 are used to select the different modes of operation of the comm demod. RECEIVE MODE switch S2 is a 2-section eight-position switch and the eight contacts of each section are connected to matrix module A45. The desired mode of operation for each position of RECEIVE MODE switch S2 is obtained by inserting a peg into the hole on the matrix module which corresponds to the desired function. Matrix module A45 can be set up in numerous configurations, but only the initial configuration is covered in the following analysis:

(1) The 21.4 MC PREDETECT BW SELECT position of matrix module A45 is associated with section A, and all other positions are associated with section B. On the 21.4 MC IF PREDETECT BW SELECT section of the matrix module, pegs are inserted into positions V1 through V4 on the 75-kHz line (terminal A), V5 on the 150 kHz line (terminal B), V6 on the 300-kHz line (terminal C), V7 on the 560-kHz line (terminal D), and V8 on the 1-MHz line (terminal E).

(*a*) With RECEIVE MODE switch S2 set in positions V1 through V4, +28 vdc is applied to the 75-kHz select diode switches in signal bandwidth select modules A5 and All. This selects 75-kHz bandpass filter A6 as the 21.4MHz if. filter.

(*b*) The remaining four positions, V5 through V8, of RECEIVE MODE switch S2 function the same as positions V1 through V4 ((a) above) except for the filter selected. Positions V5 through V8 perform filter selections as follows: V5 selects 150-kHz bandpass filter A7, V6 selects 300-kHz bandpass filter A8, V7 selects 500-kHz bandpass filter A9, and V8 selects 1-MHz bandpass filter A10.

(2) On the 1.4 MC IF PREDETECT BW SELECT section of the matrix module, a peg is inserted into the V3 position on the 4-kHz line and into positions V1, V2, and V4 through V8 on the 10-kHz line. The 10-kHz line on the matrix module has no external connections, therefore, the pegs on this line do not perform a function but are provided as spare pegs which can be used to change the configuration. When RECEIVE MODE switch S2 is set to the V3 position, +28 vdc is applied to the K1 relays in 1.4-MHz bandwidth select modules A31 and A46 (sheet 9). The +28 vdc energizes the relays which select 4-kHz bandpass filter A32 in place of 10-kHz bandpass filter A33 as the 1.4-MHz if. filter.

(3) On the 21.4 MC LOOP BW SELECT section of matrix module A45 (sheet 8), pegs are

inserted into the V1, V3, and V4 positions on the 50-kHz line. V2 position on the 30-kHz line, V5 position on the 300-kHz line, and V6, V7, and V8 positions on the 1500-kHz line.

(a) In position V2 of RECEIVE MODE switch S2, +28 vdc is applied to energize relay K1 in 21.4-MHz loop amplifier A21 (sheet 9). This selects 30-kHz loop filter A18 as the 21.4-MHz if. phase lock loop filter.

(b) When RECEIVE MODE switch S2B (sheet 8) is set to the V5 position, +28 vdc is applied to energize relay K2 in the 21.4-MHz loop amplifier A21 (sheet 9). This selects 300-kHz loop filter A49 as the 21.4-MHz if. phase lock loop filter.

(*c*) When RECEIVE MODE switch S2B (sheet 8) is set in positions V6, V7, or V8, +28 vdc is applied to energize relay K3 in 21.4-MHz loop amplifier A21 (sheet 9). This selects 1.5-MHz loop filter A20 as the 21.4-MHz if. phase lock loop filter.

(*d*) When RECEIVE MODE switch S2B (sheet 8) is set to positions V1, V3, or V4, relays K1 through K3 in 21.4-MHz loop amplifier A21 (sheet 9) are deenergized and 50-kHz loop filter A19 is selected.

(4) On the 1.4 MC LOOP BW SELECT section of matrix module A45 (sheet 8), pegs are inserted into positions V1, V2, and V4 through V8 on the 550-Hz line and V3 on the 275-Hz line.

(*a*) When RECEIVE MODE switch S2 is set to the V3 position, +28 vdc is applied to energize relay K1 in 1.4-MHz loop amplifier A40 (sheet 9). This action selects 275-Hz loop filter A41 (sheet 9) as the 1.4-MHz phase lock loop filter.

(*b*) When RECEIVE MODE switch S2 (sheet 8) is set to any position except V3, relay K1 in 1.4-MHz loop amplifier A40 (sheet 9) is deenergized and 550-Hz loop filter A42 is the selected filter for the 1.4-MHz if. phase lock loop.

(5) On the DISCR BW section of the matrix module (sheet 8), pegs are inserted into positions V1 and V2 on the 200-kHz line, V3 and V4 on the 15-kHz line, and V5 through V8 on the 2000-kHz line.

(*a*) When RECEIVE MODE switch S2 is set to either position V3 or V4, + 28 vdc is applied to relay K2 in afc and sweep module A29. This selects the output of 1.4-MHz discriminator A26 (sheet 8) as the input to operational amplifier AR1.

(*b*) When RECEIVE MODE switch S2 is set to positions V5 through V8, +28 vdc is applied to energize relay K1 in afc and sweep module A29. This selects the output of 21.4-MHz wideband discriminator A24 as the input to operational amplifier AR1.

(*c*) When RECEIVE MODE switch S2 is set to position V1 or V2, relays K1 and K2 are deenergized and the output of 21.4-MHz narrowband discriminator A25 is applied to operational amplifier AR1.

(6) On the agc section of matrix module A45, pegs are inserted into positions V1, V2, and V5 through V8 on the 21.4-MHz line, and V3 and V4 on the 1.4-MHz line.

(a) When RECEIVE MODE switch S2 is set to position V3 or V4, +28 vdc is applied to energize relay K1 in X4 frequency multiplier A28 (sheet 9) and relay K1 in relay module A48, respectively. The energized relays enable the X4 frequency multiplier and select the detected envelope output of 1.4-MHz post amplifier A34 for application to agc amplifier A22 (sheet 10) and signal detect module A23.

(*b*) When RECEIVE MODE switch S2 (sheet 8) is set to positions V1, V2, or V5 through V8, both K1 relays are deenergized which disables X4 frequency multiplier A28 and selects the detected envelope output of 21.4-MHz post amplifier A12 for application to agc amplifier A22 and signal detect module A23.

(7) On the TRACK ERROR section of matrix module A45, pegs are inserted into positions V1, V2, and V5 through V8 on the 21.4-MHz line and V3 and V4 on the 1.4-MHz line.

(*a*) When RECEIVE MODE switch S2 is set to the V3 or V4 position, +28 vdc is applied to energize relay K2 in relay module A48 (sheet 10). This selects the demodulated envelope output of 1.4-MHz am. phase detector A37 for application to am. amplifier A44 and phase lock and sweep stop module A27.

(*b)* When RECEIVE MODE switch S2 (sheet 8) is set to the V1, V2, or V5 through V8 position, relay K2 is deenergized and the output of 21.4-MHz am. phase detector A13 (sheet 9) is selected for application to the amplifier and phase lock and sweep stop circuits.

(8) On the AUDIO AMPL LOOP FREQUENCY section of matrix module A45 (sheet 8), plugs are inserted into positions V1, V2, and V5 through V8 on the 21.4-MHz line and V4 and V3 on the 1.4-MHz line.

(*a*) When RECEIVE MODE switch S2 is set to the V3 or V4 position, +28 vdc is applied to energize relay K3 in relay module A48 (sheet 9). This selects the demodulated audio output of the 1.4-MHz if. circuits which is applied to 0-30 db attenuator and audio amplifier A43 (sheet 10).

(*b*) When RECEIVE MODE switch S2

(sheet 8) is set to the V1, V2, or V5 through V8 position, relay K3 is deenergized and the output of the 21.4-MHz circuits is selected and applied to the 0-30 db attenuator and audio amplifier A43.

(9) On the DEMOD. MODE section of matrix module A45, pegs are inserted into positions V1, V2, and V5 through V8 on the fm line and V3 and V4 on the pm line.

(*a*) When RECEIVE MODE switch S2 is set to the V3 or V4 position, +28 vdc is applied to energize relay K4 in relay module A48 (sheet 9). This controls application of the demodulated audio outputs of 21.-MHz loop phase detector A16 and 1.4-MHz loop phase detector A36 and applies the demodulated audio signals to relay K3.

(*b*) When RECEIVE MODE switch S2 (sheet 8) is set to the V1, V2, or V5 through V8 position, relay K4 (sheet 9) is deenergized and the baseband outputs of 21.4/1.4-MHz loop amplifier A21 and 1.4-MHz loop amplifier A40 are selected and applied to K3.

2-58. Beacon Demodulator Operation
(fig. FO 2-2)

a. The beacon demod receives a 70-MHz signal from the if. patch panel and a 5-MHz reference frequency from the frequency standard 1A2A24 and frequency distribution unit 1A2A22. The 70-MHz signal is applied through 70-MHz bandpass filter A1 (sheet 11) to 70MHz/21.4-MHz balanced mixer A2. The 70-MHz bandpass filter has a bandwidth of 4-MHz and an attenuation of 5 db. In addition to the 70-MHz signal, 70-MHz/21.4-MHz balanced mixer A2 receives a 1-mV signal from the 48.6MHz VCO A3. The two frequencies are mixed and the difference frequency of 21.4-MHz is applied to 21.4-MHz if. preamplifier A4. The if. signal is amplified by 21.4-MHz if. preamplifier A4 and is applied to two-way power divider A35. The gain of 21.4-MHz if. preamplifier A4 is controlled by an agc voltage from agc amplifier A23 (d below). The 21.4-MHz if. preamplifier is capable of providing a gain of 50 db, but the agc voltage controls the gain over a 40 db range. One output of two-way power divider A35 is terminated by coaxial termination AT4 and the other output is applied to 21.4/1.4-MHz balanced mixer A7. The 21.4/1.4-MHz balanced mixer also receives a 20-MHz signal from X4 frequency multiplier A26. The X4 frequency multiplier receives a 5-MHz input from a 5-MHz distribution amplifier (para 2-65). The 5-MHz signal is multiplied by a factor of 4 and the resulting 20-MHz signal is applied to 21.4/1.4-MHz balanced mixer A7 and 1.4-MHz discriminator A14 (*l* below).

b. The 20-MHz and 21.4-MHz signals are mixed in 21.4/1.4-MHz balanced mixer A7 and the difference frequency of 1.4-MHz is applied to four-way power divider A8. Test point connectors J1 and J4 of four-way power divider A8 are terminated by coaxial terminations AT2 and AT3. The other two outputs are applied to 1.28-MHz post amplifier A5 (*i* below) and to the wiper arm of selector switch SID. When selector switch S1 is set to NORMAL position, the 1.4MHz if. signal is applied through 6-kHz bandpass filter A11, contacts 2 and 3 of energized relay K2 (in selector switch A12), to the 1.4-MHz if. amplifier A13 (sheet 12). Relay K2 is energized by the application of +28 vdc from contact 1 of selector switch A1A. When selector switch S1 (sheet 11) is set to the LAST DITCH BEACON position, the 1.4-MHz if. signal is applied through 600 Hz bandpass filter A9, contacts 2 and 4 of relay K1, and contacts 2 and 4 of relay K2 to the 1.4-MHz if. amplifier A13. When selector switch S1 is set to the LAST DITCH COMM position, the 1.4 MHz if. signal is applied through 3-kHz bandpass filter A10, contacts 2 and 3 of relay K1, and contacts 2 and 4 of relay K2 to 1.4-MHz if. amplifier A13. Relay K1 is energized by +28 vdc applied from contact 9 of selector switch A1A. The 1.4-MHz if. signal is amplified and detected by 1.4-MHz if. amplifier A13 (sheet 12). The 1.4-MHz if. amplifier provides three 1.4-MHz if. outputs and one detected envelope output. The detected envelope output is applied to agc amplifier A23 *(d* below), signal detect module A22 (*c* below), and am. amplifier A33. The detected envelope signal is amplified by am. amplifier A33 and used as a tracking error signal (for forced-track operation only). The three 1.4-MHz if. outputs of 1.4-MHz if. amplifier A13 are applied through part of X2 frequency multiplier A37 to the 2.8-MHz loop phase detector A15 (*e* below), through part of X2 frequency multiplier A37 to the 2.8-MHz loop phase detector A16 (*h* below), and to the 1.4-MHz discriminator A14 (*l* below) respectively.

c. The detected envelope signal input to signal detect module A22 (*b* above) is applied to dc amplifier AR1 which functions as a level detector. When the envelope signal exceeds the preset bias level of AR1, the output of the amplifier triggers a 4-second module monostable multivibrator. When selector switch S1 is set to the NORMAL position, +28 vdc is applied to energize relay K3 (fig. FO 2-5, sheet 6). This selects the preset (for normal operation) bias level for AR1. When selector switch S1 is set to the LAST DITCH

BEACON position, relay K3 deenergizes and relay K4 is energized. This lowers the bias level of AR1 and ensures that when the detected envelope signal is low in amplitude the multivibrator will be triggered. The 4-second pulse output of the monostable multivibrator energizes relay K2 (sheet 12) and is applied to an OR gate in phase lock detect and sweep stop logic A21. A 4-second signal detect indication signal is applied to the antenna control circuits from the contacts of relay K2. When the 4-second pulse is applied to the OR gate in phase lock detect and sweep stop logic A21, the output of the dc amplifier energizes the sweep stop relay K3. A ground is applied through the closed contacts of the sweep stop relay to pin 1 of connector J1 of afc and sweep module A34 (sheet 11). This ground inhibits the sawtooth oscillator in the sweep generator circuit. If the 1.4-MHz if. phase lock loop has phase locked prior to the depletion of the 4-second pulse, the output of the phase lock detect circuit to the phase lock detect and sweep stop logic A21 assumes control of the sweep stop relay (*h* below). The sweep stop relay remains energized provided that phase lock is maintained.

d. The detected envelope output of 1.4-MHz if. amplifier A13 (*b* above) is applied to age amplifier A23 (sheet 11). This signal is amplified by dc amplifier AR1 and applied to SIGNAL STRENGTH meter M1, the antenna control circuits, and to servo operational amplifier AR2 in age amplifier A23. The output of AR2 is applied to 21.4-MHz if. preamplifier A4 (*a* above). The high gain of age amplifier A23 insures that the if. output of the 21.4-MHz if. preamplifier remains constant over a 40-db range.

e. The 1.4-MHz if. output from J3 of 1.4-MHz if. amplifier A13 (*b* above) is applied to X2 frequency multiplier A37 (sheet 12), where the frequency is doubled, and then routed to 2.8-MHz loop phase detector A15. The 2.8-MHz loop phase detector is part of the phase lock loop consisting of 2.8-MHz loop amplifier A20, 1.4-MHz VCXO A18, three-way power divider A24, part of X2 multiplier A37, and 90° phase shifter A17. The 2.8-MHz loop phase detector A15 receives two inputs: the 2.8-MHz if. signal from X2 multiplier A37 and a 2.8-MHz 90° reference signal from 90° phase shifter A17. The 90° reference signal is generated by 1.4-MHz VCXO A18, doubled in frequency, and then applied to the 90° phase shifter A17. Provided the 2.8-MHz signals are in phase, the output of the 2.8-MHz loop phase detector is zero. If one of the 2.8-MHz reference signals changes frequency, a dc error voltage, proportional to the phase difference between the two signals, is produced at the output of 2.8-MHz loop phase detector A15.

f. The polarity of the dc error voltage is dependent upon the direction of phase error. The dc error voltage is applied through 275-Hz filter A19 to the input of dc amplifier AR1 in 1.4-MHz loop amplifier A20. In the absence of a dc error input, dc amplifier AR1 is biased at a dc level which produces a corresponding output dc level that establishes the frequency of 1.4-MHz VCXO A18. When the dc error voltage is combined with the bias voltage at the input to dc amplifier AR1, the output de level of AR1 is changed, which produces a corresponding change in the 1.4-MHz VCXO frequency. The output frequency of 1.4MHz VCXO A18 is changed in the direction necessary to correct the phase error at 2.8-MHz phase detector A15. In this manner, the 1.4-MHz VCXO A18 is phase locked to the incoming 2.8MHz if. signal. The 275-Hz filter A19 is connected across dc amplifier AR1 in 2.8-MHz loop amplifier A20. The output of dc amplifier AR1 is applied as feedback through the 275 Hz filter to the input of AR1. The 275 Hz filter establishes the bandwidth of the phase lock loop by controlling the bandwidth of dc amplifier AR1.

g. The 1.4-MHz output of 1.4-MHz VCXO A18 is applied to three-way power divider A24. Test point connector J1 of three-way power divider A24 is terminated by coaxial termination AT1 and the other two inputs are applied through X2 multiplier A37 to 90° phase shifter A17 and to 1.28-MHz/120-kHz balanced mixer A25, respectively. The 90° phase shifter A17 provides two outputs which are 90° out-of-phase. The 2.8-MHz 45° phase input is inductively phase shifted +45° to provide a 2.8-MHz 0° phase output which is applied to 2.8-MHz loop phase detector A16. The 2.8-MHz 45° phase input is also capacitively phase shifted-45° to provide a 2.8-MHz 90° phase output which is applied to 2.8-MHz loop phase detector A15.

h. The 1.4-MHz if. output from J2 of 1.4-MHz if. amplifier A13 (b above) is routed to X2 frequency multiplier A37 (sheet 12) where the frequency is doubled. The 2.8-MHz loop phase detector A16 receives the 2.8-MHz 0° phase signal from 90° phase shifter A17, and the 2.8-MHz IF signal from X2 frequency multiplier A37. The 2.8-MHz loop phase detector A16 produces a coherent dc voltage of approximately +1 volt when the 1.4-MHz phase lock loop is locked. When the loop is not locked, the two input signals are not in phase and the coherent dc voltage is not produced. Any modulation (am. or fm.) that is present on the 2.8-MHz signal input to 2.8 MHz loop phase detector A16, will cause the coherent dc voltage to vary at an audio rate

coherent dc voltage to vary at an audio rate and produce an envelope signal which contains the 25-Hz tracking signal. The envelope signal is applied to phase lock detect and sweep stop logic A21, am. amplifier A33, and audio amplifier A32. The envelope signal is amplified by audio amplifier A32 and the output is applied to the baseband amplifier (sheet 18) as the aural acquisition aid signal. The am. amplifier A33 amplifies the 25-Hz tracking signal and applies it to the antenna control circuits as a tracking error signal. The envelope signal input to phase lock detect and sweep stop logic A21 is applied to a dc amplifier AR1 which functions as a level detector. When the envelope input exceeds the level detector reference level, the output of the level detector is clamped at a maximum negative voltage. This negative voltage energizes beacon track relay K1, phase lock detect relay K2 and +28 volts is applied through relay K1 contacts to illuminate BEACON TRACK ACQ indicator lamp DS6. Relay K2 contacts apply a phase lock detect indication to the antenna control circuits. The negative output level of AR1 is applied as one input to an OR gate. The output of the OR gate biases a dc amplifier AR2 which energizes the sweep stop relay K3. When the sweep stop relay is energized, a ground is applied to afc and sweep amplifier A34 (*m* below). This ground prevents the sweep generator circuit from producing a sweep. The long time constant (approximately 2 seconds) of AR2 prevents the sweep stop relay from deenergizing if the phase lock loop momentarily loses a lock condition due to very low signal levels.

i. The 1.28-MHz post amplifier A5 (sheet 11) receives the 1.4-MHz if. signal from four-way power divider A8 (*b* above). The 1.28-MHz post amplifier A5 is a narrowband amplifier that amplifies the beacon identification signal which is centered at 1.28 MHz. The 1.28-MHz output signal is applied through 50-kHz bandpass filter A6 (sheet 12) to 1.28-MHz/120-kHz balanced mixer A25. The 1.28-MHz/120-kHz balanced mixer A25 also receives the 1.4-MHz 45° output from three-way power divider A24. The two frequencies are mixed and the resulting difference frequency is applied through 120-kHz filter/ amplifier A27 to 120-kHz loop phase detector A28. Test point connector J3 of the 120-kHz filter/amplifier is terminated by coaxial termination AT10.

j. The satellite identification circuit is basically a phase lock loop which is comprised of 120 kHz loop phase detector A28, ID sweep, loop filter, and acquisition circuit A29, 480 kHz VCXO A31, and ID four-to-one countdown and quadrature circuit A30. Initially or prior to a phase lock condition, ID sweep, loop filter and acquisition circuit A29 is producing a sawtooth sweep voltage that is applied to 480-KHz VCXO A31. This causes the 480-kHz VCXO to sweep around the center frequency of 480 kHz. The output of the 480-kHz VCXO is applied to ID four-to-one countdown and quadrature circuit A30. The input frequency to the ID four-to-one countdown circuit is divided by 4 and applied to a +90° quadrature circuit, to one of the phase detectors in 120-kHz loop phase detector A28, and to connector J1 of the beacon demodulator. The output of the +90° quadrature circuit is applied to the other phase detector in the 120kHz loop phase detector A28. Both phase detectors receive the 120-kHz phase 0° signal from 120-kHz filter/amplifier A27.

k. The phase detector which receives the two 0° signals (*j* above) produces a coherent dc level output when the two signals are in phase. The phase detector which receives the 0° and 90° signals produces a null or zero output when the two signals are in phase. As the swept frequency from the four-to-one countdown circuit approaches an in phase condition with the if. input, a coherent dc level is produced which represents the detected envelope. The coherent dc level is applied to a level detector in the ID sweep, loop filter, and acquisition circuit A29. When the dc level exceeds the reference level of the level detector, the output of the level detector energizes relay K1 to inhibit the generation of the sawtooth sweep voltage. This allows 480kHz VCXO A31 to produce a frequency corresponding to the satellite identification. At this time, the output of the other phase detector is nearing zero (in-phase condition). Any phase error that exists, produces a dc voltage that is applied through the loop amplifier to 480-kHz VCXO A31 and causes the VCXO to shift frequency and null the output of the phase detector. In this manner, 480-kHz VCXO A31 is phase locked to the incoming 120-kHz signal. When the loop is phase locked and relay K1 is energized by the level detector output, +28 vdc is applied through the relay contacts to illuminate BEACON SIGNATURE DISPLAYED indicator lamp DS7.

l. The 1.4-MHz discriminator A14 (sheet 11) receives a 20-MHz reference frequency from the X4 frequency multiplier A26 (*a* above) and a 1.4-MHz if. signal from 1.4-MHz if. amplifier A13 (*b* above). The two signals are mixed to produce the 21.4-MHz signal which is applied to the crystal discriminator circuit. If the incoming 1.4-MHz if. frequency changes, the crystal

discriminator produces a dc error voltage proportional to the amount of frequency shift. This dc error voltage is applied to pin 2 of connector J2 of afc and sweep amplifier A34.

m. Afc and sweep amplifier A34 (sheet 11) receives the output of 1.4-MHz discriminator A14 (*l* above) and a sweep stop signal from phase lock detect and sweep stop logic A21 (*h* above). When the afc loop is locked, the dc error voltage output of 1.4-MHz discriminator A14 is applied to dc amplifier AR1 in afc and sweep amplifier A34. The dc error voltage is amplified by AR1, an amplifier in the sweep generator circuit, and dc amplifier AR3. The output of amplifier AR3 is applied to 48.6-MHz VCO A3 to change the 48.6-MHz frequency in a direction and by an amount necessary to return the 1.4-MHz discriminator A14 output to zero. At this time, the sawtooth oscillator in the sweep generator circuit of afc and sweep amplifier A34 is disabled by a ground at pin 1 of connector J1 applied from phase lock detect and sweep stop logic A21 (h above).

n. If the afc loop unlocks and stays unlocked in excess of 2 seconds, the ground is removed from pin 1 of connector J1 (*m* above) and the sweep generator circuit starts producing a sweep voltage that is amplified by dc amplifier AR3 and then applied to 48.6-MHz VCO A3. The sawtooth sweep voltage is centered on the dc level which controls the 48.6-MHz frequency and causes it to vary above and below 48.6-MHz. When the received signal is again of sufficient strength, an increase is produced in the detected envelope input signal to signal detect logic A22 (sheet 12) and the afc loop will again be locked. The signal detect logic A22 then applies a 4-second pulse to phase lock detect and sweep stop logic A21, energizing the sweep stop relay K3 which, in turn, applies a ground to pin 1 of connector J1 of afc and sweep amplifier A34 (sheet 11). This ground inhibits the sweep generator circuit and the output of 1.4-MHz discriminator A14 assumes control of 48.6-MHz VCO A3. Assuming that the afc loop has locked and brought the received signal into the center of the if. passband, the 21.4-MHz if. phase lock loop will phase lock almost instantaneously. When the phase lock loop locks, the demodulated envelope input to phase lock detect and sweep stop logic A21 (sheet 12) causes the phase detect circuit to assume control of the sweep stop relay K3.

o. When TUNING MODE switch S2 (sheet 11) is set to the afc position, the output of the sweep generator circuit of afc and sweep amplifier A34 is applied to VCO TUNING meter M2. VCO tuning meter M2 is calibrated in kHz and indicates the amount of frequency deviation that the 48.6-MHz frequency is from center frequency. When TUNING MODE switch S2 is set to the MAN position, VCO TUNING meter M2 is disconnected from the sweep generator circuit and a ground is applied through contacts 1 and 2 of switch S2 to disable the amplifier in the sweep generator circuits. VCO MANUAL TUNING COARSE R1 and FINE R2 potentiometers are part of a voltage divider network connected between +28 vdc and -28 vdc. Potentiometers R1 and R2 control the output level of de amplifier AR3. This in turn controls the frequency of 48.6-MHz VCO A3 and causes the frequency to either increase or decrease depending upon the direction that the potentiometers are rotated.

p. When TUNING MODE switch S2 is set to the afc position, and selector switch S1 is set to the NORMAL position, the sweep output of the sweep generator circuits will sweep 48.6-MHz VCO A3 +150 kHz. When selector switch S1 is either in the LAST DITCH BEACON or LAST DITCH COMM position, +28 vdc is applied to energize relays in the sweep generator and the signal detect module A22. When the relays energize, the sweep output of the sweep generator is reduced in amplitude and the 48.6-MHz VCO is swept +15 kHz. The bias level in the signal detect module A22 is also adjusted (*c* above).

2-59. Composite Voice and Teletypewriter Receive Signal Paths

(fig. FO 2-2, sheets 14 and 15)

The baseband outputs of comm demods 1A3A3 and 1A3A5 are applied to the baseband patch panel on DEMODULATOR 1 LINE jacks J13 and J14 and DEMODULATOR 2 LINE jacks J15 and J16, respectively. LINE jacks J13 and J14 are normalled-through to COMM-AMPL EQUIP jacks J37 and J38 and MON jacks J61 and J62. If the output of comm demod number 2 is desired in place of comm demod number 1, a patch cord is inserted into DEMODULATOR 2 LINE jacks J15 and J16 and COMM AMPL EQUIP jacks J37 and J38. The output of EQUIP jacks J37 and J38 is applied through baseband differential amplifier A46 and the wiper arm of COMP potentiometer R27B to baseband operational amplifier A41. Potentiometer R27 is used to control the gain of the amplifier by controlling the amount of feedback. The output of baseband operational amplifier A41 is applied to EMPHASIS SELECT switch S7 and to meter calibrate potentiometer R13. EMPHASIS SELECT switch S7 is used to select

one of six available deemphasis networks. The selected deemphasis network, deemphasizes the higher baseband frequencies which were accentuated at the sending station and improves the signal-to-noise ratio. The deemphasis action is accomplished by connecting the selected deemphasis network across baseband operational amplifiers A47 and A42. The deemphasis network controls the feedback to the baseband operational amplifiers and thus controls the frequency response of the amplifiers. The output of baseband operational amplifier A42 is applied through baseband power amplifier A48 to 3995 potentiometer R24, 3805 potentiometer R25, and VOICE potentiometer R26. VOICE potentiometer R26 is used to adjust the baseband input level to baseband power amplifier A26. The output of baseband power amplifier A26 is applied to meter calibrate to potentiometer R14 and through baseband isolation transformer A29 to COMM AMPL VOICE LINE jacks J17 and J18. The metering circuit associated with meter calibrate potentiometer R14 is covered in paragraph 2-63. LINE jacks to J17 and J18 are normalled-through to VOICE MODE SEL SW EQUIP jacks J41 and J42 and 3, MON jacks J65 and J66. The baseband signal is applied from EQUIP jacks J41 and J42 to wiper arms C1 and C2 of MODE SELECT switch S5.

2-60. Wideband Multiplex Receive Signals
(fig. FO 2-2, sheet 15)

With MODE SELECT switch S5 in the V5 position, the baseband signal is applied through section C of the switch to VOICE MODE SEL SW WIDEBAND jacks J19, J20 and MON jacks J67 and J68 LINE jacks J19 and J20 are normalled-through to WIDEBAND EXT EQUIP jacks J43 and J44. The signal at EQUIP jacks J43 and J44 is applied through fuses F103 and F104 and WIDEBAND ext pair J5 to the external user.

2-61. Voice Receive Signal Path
(fig. FO 2-2)

For purpose of this manual, the common voice signal path from MODE SELECT switch S5 (sheet 15) is identified as user voice/orderwire voice (*a* below). The external user signal path is identified as user voice (*b* below), and the order-wire user signal path is identified as orderwire (O/W) voice (*c* below).

a. With MODE SELECT switch S5 set to the V1 position, the baseband signal is applied to terminals 7 and 8 of voice/tty filter FL6 and to VOICE/TTY FIL TP EQUIP jacks J37 and J38. Filter FL6 is a two section filter which separates last ditch 1,275-Hz teletypewriter signal from the baseband signal. One section passes frequencies between 1,180 and 1,370 Hz and plies the 1,275-Hz teletypewriter output at terminals 3 and 4 to VOICE/TTY FIL TG LINE jacks J23 and J24. The other section of filter FL6 passes frequencies between 300 and 1,180 Hz and between 1,370 and 3,500 Hz. The output at terminals 1 and 2 of filter FL6 is applied to terminals 2 and 8 of MODE SELECT switch S5D d to VOICE/TTY FIL LINE LINE jacks J13 and J14 and MON jacks J61 and J62. With MODE SELECT switch S5 set to the V2 position, the baseband signal is applied to terminals 7 and 8 of truncated filter FL4 and to TRUNTED FIL EQUIP jacks J39 and J40. Filter FL4 passes frequencies between 300 and 1,800 and the output at terminals 1 and 2 is applied terminals 3 and 9 of MODE SELECT switch S5D and to TRUNCATED FIL LINE jacks J15 d J16. With MODE SELECT switch S5 set to the V3 position, the baseband signal is applied to terminals 7 and 8 of normal voice filter FL2 and NORMAL FIL EQUIP jacks J41 and J42. Filter FL2 passes frequencies between 300 and 3,400 Hz and the output is applied to terminals 4 and 10 of switch S5D and to NORMAL FIL LINE jacks J17 and J18 and MON jacks J65 and 3. The selected voice signal is applied from switch S5D to VOICE MODE SEL SW LINE jacks J13 and J14 and MON jacks J61 and J62. Line jacks J13 and J14 are normalled-through to ECHO SUPPR RECEIVER EQUIP jacks J37 and J38. The voice signal at EQUIP jacks J37 and J38 is applied through echo suppressor receiver A9 (sheet 16) to ECHO SUPPR RECEIVER LINE jacks J15 and J16. For a fourwire user, the echo suppressor receiver is received from the receive voice path by inserting a patch cord into VOICE MODE SEL SW LINE jacks J13 and J14, and VOICE SOURCE SEL SW QUIP jacks J39 and J40. For an analysis of ho suppression refer to paragraph 2-67. The signal at ECHO SUPPR RECEIVER LINE jacks J15 and J16 is normalled-through to VOICE SOURCE SEL SW EQUIP jacks J39 and J40 (sheet 18) to VOICE selector switch S1.

b. When VOICE selector switch S1 is set to the USER position, the voice signal is applied to VOICE SOURCE SEL SWITCH USER-LINE jacks J19 and J20 and MON jacks J67 and J68. LINE jacks J19 and J20 are normalled-through USER AMP EQUIP jacks J43 and J44. The signal at EQUIP jacks J43 and J44, is applied to baseband differential amplifier A16. The amplified output of the differential amplifier is applied to meter

calibrate potentiometer R4 and LEVEL potentiometer R17B. Potentiometer R17B is used to adjust the voice level input to baseband operational amplifier A21. Potentiometer R17A is used to control the gain of the amplifier by varying the amount of feedback. The output of baseband operational amplifier A21 is amplified by baseband power amplifier A15 and is applied to baseband setup transformer A20 and to meter calibrate potentiometer R3. The output of baseband setup transformer A20 is applied to USER AMP LINE jacks J21 and J22 and MON jacks J69 and J70 (sheet 19). LINE jacks J21 and J22 are normalled-through USER VOICE NO. 2 EQUIP jacks J45 and J46. The signal at EQUIP jacks J45 and J46 is applied through 0- to 4-kHz FL2 to user 2 RCV OUT terminals E3 and E4. From E3 and E4 the user voice signal is applied to the external user landlines.

c. When voice source selector switch S1 is set to the ORDERWIRE position, the orderwire voice signal is applied to VOICE SOURCE SEL SWITCH O/W LINE jacks J17 and J18 and MON jacks J65 and J66. LINE jacks J17 and J18 are normalled-through to ORDERWIRE AMP EQUIP jacks J41 and J42. The signal at EQUIP jacks J41 and J42 is applied to selector switch S Selector switch S3 also receives the aural acquisition aid signal that is applied from the beacon demod through baseband isolation transformer A54 to terminals 1 and 4 of switch S3. The selected signal is applied to baseband differential amplifier A59 (sheet 18). The amplifier output of baseband different amplifier A59 is applied to meter calibrate potentiometer R6 and LEVEL potentiometer R19A. Potentiometer R19A is used to adjust the input signal level to baseband operational amplifier A55. Potentiometer R19B is connected across baseband operational amplifier A55 and is used to control the gain of the amplifier by controlling the amount of feedback. The output of baseband operational amplifier A55 is amplified by baseband power amplifier A60 and is applied to handset assembly HS1.

2-62. Teletypewriter Receive Signal Paths
(fig. FO 2-2)

For purposes of this manual, the external user tty signal path is identified as user tty (*a* below) and the terminal user tty signal path is identified as orderwire tty (*b* below). Either the user or orderwire may operate in the last ditch (*c* below) mode, but the alternate mode will be rendered inoperative. For example, if the user is rating in last ditch, the orderwire mode must off.

a. The baseband signal present at 3995 potentiometer R24 is amplified by baseband power amplifier A49 and applied to COMM AMP 3995 LINE jacks J19 and J20 and MON jacks J67 and J68. LINE jacks J19 and J20 are normalled-through to 3995 C/S CONVERTER EQUIP jacks and J44. The signal at EQUIP jacks J43 and is applied through baseband isolation transformer A17A10 (sheet 15) to connector 24 of frequency shift converter A6 (sheet 16). A filter at the input of frequency shift converter passes only the 3995-Hz teletypewriter signal and rejects the remaining portions of the baseband signal. The 3,995-Hz teletypewriter signal is applied as an output from connector 21 to meter calibrate potentiometer R12. Frequency shift converter A6 converts discrete mark and space tones into corresponding dc binary signals. Output connectors P1-7 and P1-20 part of a series dc loop. The mark and space puts are produced by the opening and closing set of relay contacts within the keyer converter which connects pins 7 and 20 of connector or a mark and opens the circuit between pins and 20 for a space. The dc user tty signal out of the 3995-Hz frequency converter A6, is applied to contacts 8 and 10 of the TTY MODE ER switch S4. With the TTY MODE USER switch S4 set to NORMAL, contacts 7, 8, 9, and are made, and the user tty signal is applied to TTY SEL SW 3995 Hz RX LINE jack J2A and MON jack J28 on the teletypewriter patch panel. LINE jack J2A is normalled-through to RX LIU-1 3995 USER EQUIP jack J2B. The user signal at EQUIP jack J28 is applied to J2 pins X and Y on the line isolation unit, line isolator-1 (LIU-1). LIU-1 provides dc isolation between the in-station and out-station signals. LIU/1 also converts in-station ± 6 vdc polar signals to signals compatible with the users equipment. The output of LIU/1 is applied from J3 pins g and h on the line isolation unit through filter FL34 and fuses F67, and F68 and LIU/1 RCV OUT terminals E67 and E68 to the external user.

b. The baseband signal present at the wiper arm of 3805 potentiometer R25 (sheet 14) is amplified by baseband power amplifier A22 and applied to COMM AMPL 3805 C/S LINE jacks and J22 and MON jacks J69 and J70. LINE jacks J21 and J22 are normalled-through to 3805 CONVERTER EQUIP jacks J45 and J46. The signal at EQUIP jacks J45 and J46 is lied through baseband isolation transformer to connector P1-24 of frequency shift converter A5. A filter at the input or the

frequency shift converter passes only the 3,805 Hz teletypewriter signal and rejects the remaining portions of the baseband signal. The 3,805-Hz teletypewriter signal is applied as an output through connector P1-21 to meter calibrate potentiometer R11. Frequency shift converter A5 converts discrete mark and space tones into corresponding dc binary signals. Output connectors P1-7 and P1-20 are part of a series dc loop and operative in an identical manner as described in (*a* above). The dc orderwire tty signal output of the 3805 Hz frequency converter A5 is applied to contacts 8 and 10 of TTY MODE ORDERWIRE switch S3. With the TTY MODE ORDERWIRE switch S3 set to NORMAL contacts 7, 8, 9, and 10 are made and the orderwire tty signal is applied to TTY SEL SW 3805 RX LINE jack J4A, and MON jack J30 on the teletypewriter patch panel LINE jack J4A is normalled-through to LIU-2 3805 Hz OW RX EQUIP jack J4B. The orderwire tty signal at EQUIP jack J4B is applied to J2 pins r and s on the line isolation unit, line isolator-2 (LIU-2). LIU-2 operates in an identical manner as LIU-1 described in (*a* above). The output of LIU-2 is applied from J3, pins a and b on the line isolation unit to filter FL36 and fuses F71 and F72, and LIU-2 RCV OUT terminals E71 and E72.

NOTE

In the event the UGC-77 teletypewriter terminal console 1A3A23 is to be used as the orderwire user, the orderwire user tty signal present at TTY SEL SW 3805 Hz RX LINE jack must be patched to the RX UGC-77 KEYBD PRINTR EQUIP jack J10B. The signal present at EQUIP jack J10B is applied through connector J3 pins J and H to the UGC-77 teletypewriter terminal console 1A3A23.

c. The 1275-Hz last ditch tty signal is applied from pins 3 and 4 of voice/tty filter FL6 (sheet 15) through VOICE/TTY FIL TG LINE jacks J23 and J24, 1275 C/S CONVERTER EQUIP jacks J47 and J48, and baseband isolation transformer A11 to frequency shift converter A4. A filter at the input of frequency shift converter A4 passes only the 1275-Hz teletypewriter signal and rejects all others. Frequency shift converter A4 converts discrete mark and space tones into corresponding dc binary signals. Output pins 7 and 20 of connector P1 are part of a series dc loop. The mark and space outputs are also produced by the opening and closing of a set of relay contacts within the frequency shift converter which connects pin 7 to 20 for a mark and opens the circuit between 7 and 20 for a space. The last ditch tty frequency shift converter A4 an be substituted for either user tty frequency shift converter A6 or orderwire tty frequency shift converter A5 by setting TTY-MODE USER witch S4 or TTY-MODE O/W switch S3 to LAST DITCH.

(1) When TTY MODE USER switch S4 is set LAST DITCH position, the output of the 3995 z frequency converter is inhibited by open contacts 7, 8, 9, and 10. The dc output of the 1275 Hz frequency converter A4, which is normalled trough KEYER CONV LINE jack J4A, MON jack J34 and RX TTY SEL SW 1275 Hz RX EQUIP jack J8B, is applied through closed contacts 1, 2, 5, and 6 to the TTY SEL SW 3995 Hz X LINE jack J2A. The LAST DITCH signal resent at the LINE jack J2A is further processed in an identical manner as the user 3995 Hz signal described in (*a* above).

(2) When TTY MODE ORDERWIRE switch 3 is set to LAST DITCH position, the output of the 3805 Hz frequency converter is inhibited by pen contacts 7, 8, 9, and 10. The dc output of the 275 Hz frequency converter A4, which is normalled-through KEYER CONV LINE jack 4A, MON jack J34 and RX TTY SEL SW 1275 Hz RX EQUIP jack J8B, is applied through closed contacts 1, 2, 5, and 6 of the TTY SEL SW 3995 Hz RX LINE jack J2A. The LAST DITCH signal present at LINE jack J2A is further processed in an identical manner as the user 3995 Hz signal described in (*a* above).

2-63. Baseband Metering Circuits (Receive)

(fig. FO 2-2)

Receive line amplifier meter select switch S6 sheet 14) receives four different inputs. The voice signal present at the wiper arm of meter calibrate potentiometer R14 is applied to terminal (VOICE position) the 3,805 Hz orderwire teletypewriter signal present at the wiper arm meter calibrate potentiometer R11 is applied terminal 2(3805 position); the 3,995-Hz user teletypewriter signal present at the wiper arm meter calibrate potentiometer R12 is applied terminal 3 (3995 position); and the composite baseband signal present at the wiper arm of potentiometer R13 is applied to terminal 4 (COMP position).

a. The selected signal to be monitored is applied to baseband operational amplifier A23 and the amplified output is applied through meter compensation network A27 to RECEIVE LINE AMPL vu meter M3. The meter compensation network provides meter compensation so that identical meters can be used in various circuits and

can be calibrated to indicate O vu for a wide range of input signal levels. The compensation network also provides meter, protection by ensuring that the output to the meter does not exceed a safe level. Potentiometers R11 through R14 are adjusted for a zero meter indication when the input signal is at the proper level.

b. The user voice signal present at the wiper arm of meter calibrate potentiometer R4 (sheet 18), is applied through the RECEIVE IN position of USER LINE AMPL switch S1 to baseband operational amplifier A18. The user voice signal present at the wiper arm of meter calibrate potentiometer R3, is applied through the RECEIVE OUT position of switch S1 to baseband operational amplifier A18. Baseband operational amplifier A18 amplifies the selected signal and the output is applied through meter compensation network A13 to USER LINE AMPL LEVEL meter M1. The meter compensation network provides meter compensation so that identical meters can be used in various circuits and can be calibrated to indicate O vu for a wide range of input signal levels. The compensation network also provides meter protection by ensuring that the output to the meter does not exceed a safe level. Potentiometers R3 and R4 are adjusted for a zero meter indication when the input signal is at the proper level.

c. The orderwire voice signal present at the wiper arm of meter calibrate potentiometer R6, is applied through the RECEIVE position of ORDERWIRE AMPL switch S2 to baseband operational amplifier A53. The output of baseband operational amplifier A53 is applied through meter compensation network A58 to ORDERWIRE AMPL LEVEL meter M2. Meter compensation network A58 is identical to that discussed in *b* above. Potentiometer R6 is adjusted for a zero meter indication when the input signal is at the proper level.

2-64. 1 kHz Tone Receive Circuit
(fig. FO 2-2, sheet 15)

With MODE SELECT switch S5 in the TEST position, the baseband signal is applied to a 1 kHz peaking amplifier stage comprised of baseband operational amplifier A5 and baseband filter transformer A4. The output of the peaking amplifier is applied through switch S5D to VOICE MODE SEL SW LINE jacks J13 and J14. This test circuit is used in conjunction with the 1 kHz test tone generation circuits discussed in paragraph 2-10.

2-65. Reference Frequency Generation

a. The reference frequency generation circuits provide accurate, stable mixing and timing signals to OCV functions and other major units in the AN/TSC54. These circuits are comprised of the cesium beam frequency standard, the frequency distribution unit, and two distribution amplifiers.

b. The frequency distribution unit (fig. FO 2-2, sheet 19) consists of the FE-12 frequency standard filter FL1, coaxial switch assembly K1, K2 and K3, two-way power divider CP3 and two limiter amplifiers AR1 and AR2. The cesium beam frequency standard supplies three inputs, 1 MHz, 5 MHz and 100 MHz to the frequency distribution unit through the coaxial switch assembly. The 100 kHz from the coaxial switch assembly is applied directly to the AN/TSC-54 modulator unit, where it is used to phase lock the 10-MHz VCO. The 1-MHz and 5-MHz signals from the coaxial switch assembly are routed through limiter amplifiers AR1 and AR2, respectively to the H.P. 5087A distribution amplifier. The cesium beam standard also applies a one-pulse-per-second signal directly to the time transfer unit. In the event the cesium beam frequency standard fails, the coaxial switch assembly can bring the FE-12 frequency standard on line by depressing S1 (XTAL STD) on the control panel FREQ RE SELECT switch.

c. The FE-12 frequency standard applies a 100-kHz signal through the-coaxial switch assembly to the AN/TSC-54 modulator and a 1-MHz signal through the coaxial switch assembly to limiter amplifier AR1. The 5-MHz signal from the FE-12 frequency standard is applied through filter FL1 and the two-way power divider CP3 to the coaxial switch assembly. FL1 has a 3 db bandwidth of 300 Hz to provide the necessary attenuation to the unwanted sidebands. The two-way power divider divides the 5-MHz signal into two outputs. One output is applied through the coaxial switch assembly to limiter amplifier AR2. The other output is made available at the frequency distribution front panel (5 MHz XTAL OUTPUT connector) for calibration of the FE-12 frequency standard.

d. The HP 5087A distribution amplifier provides multiple 1-MHz and 5-MHz outputs for application to major units in the AN/TSC54. Three 5-MHz outputs are applied to the beacon demod and comm demods 1 and 2, respectively, where they are used as mixer reference frequencies. One 5-MHz output is applied to the time transfer unit where it is used as a clock frequency. The frequency distribution amplifier also supplies a 1-MHz and 5-MHz signal for application to the Comtech Distribution Amplifier (A8) which supplies basic

frequency inputs to the frequency synthesizers (fig. FO 2-1, sheets 7 and 8). The AN/URC-61 utilizes a 5-MHz output from the distribution amplifier as a vco reference frequency.

2-65.1 OBN Monitor Panel
(fig. FO 2-2, sheet 14.1).

The OBN monitor panel provides an on-line indication of the received signal quality for a maximum of eight channels. The eight signals are received from the AN/TCC-79 via external signal distribution panel 1A10 and are applied to OBN monitor panel 1A3A24 at J1 over cable W601. The signal to be monitored is selected by a front panel CIRCUITS switch. A panel mounted TTNR meter (MA1) indicates signal quality. When the signal on the monitored channel goes out of tolerance, a visual alarm lights and an audio alarm sounds.

2-66. Radio Communication Subsystem AN/ URC-61 (Receive)
(Fig. FO 2-2, sheet 13)

The AN/URC-61 contains the necessary demodulation and baseband equipment to extract the voice and teletypewriter signals from the 70 MHz carrier. When the AN/URC-61 is to be used the receive signal from the appropriate DOWN CONV jack must be patched through the equalizer couplers CP12 and CP18 to the URC-61 jack coupler CP17 on the communication patching panel. The signal paths are described in *a* through *d* below.

a. The user voice outputs at pins A and B of connector P11 of Radio Communication Subsystem AN/URC-61 is applied to the vf baseband patch panel. At the vf baseband patch panel, the user voice output is applied to URC-61 RX-1 VOICE LINE jacks J13 and J14 and MON jacks J61 and J62. LINE jacks J13 and J14 are normalled-through the USER VOICE NO. 5 EQUIP jacks J37 and J38. From EQUIP jacks J37 and J38, the user voice signal is applied through 0- to 4-kHz filter FL5 and URC-61 5 RCV 1 OUT terminals E9 and E10 to the external user.

b. The user voice output at pins n and g of connector P11 is applied to the vf baseband patch panel. At the vf baseband patch panel, the user voice outputs to URC-61 RX2 VOICE LINE jacks J17 and J18 and MON jacks J65 and J66. LINE jacks J17 and J18 are normalled-through to USER VOICE NO. 6 EQUIP jacks J41 and J42. The user voice signal at EQUIP jacks J41 and J42, is applied through 0 to 4 kHz filter FL6 and URC-61 6 RCV 2 OUT terminals E11 and E12 to the external user.

c. The digital data output at pins s and r of connector P11 is applied to the teletypewriter patch panel. At the teletypewriter patch panel, the digital data output is applied to DIG DATA RX1 LINE jack J16A and MON jack J42. LINE jack J16A is normalled-through to RX1 DIG DATA EQUIP jack J16 B. From EQUIP jack J16B the digital data signal is applied to DIG DATA RX1 OUT terminals E85 and E86 to the external user.

d. The digital data clock output at coaxial connector P11 is applied to the teletypewriter patch panel. At the patch panel, the digital data clock output is applied to RX1 CLOCK LINE jack J1A and MON jack J44. LINE jack J18A is normalled-through to RX1 CLOCK EQUIP jack J18. From the EQUIP J18B jack the RX1 clock signal is applied to DIG DATA CLOCK RX1 terminals E77 and E78 to the external user.

2-67. Analysis of Echo Suppression
(fig. FO 2-2, sheet 15)

One transmitter and one receiver echo suppressor combination is used at each end of the communication link, and each combination is identical to the other. The echo suppressors are essentially speech operated devices with two modes of operation. Mode 1 is unidirectional and mode 2 is bidirectional. Mode 1 involves the case in which the voice transmitted at one terminal is being received at another. Under this condition, the transmitted voice echo will be suppressed or attenuated by more than 60 db. Mode 2 operation is when voice signals are transmitted at both terminals of the communications link simultaneously. During mode 2 operation, echoes are only partially suppressed, but are difficult to detect because of the higher amplitude voice signals and their sidetones. With each combination of echo suppressors, a disabler unit is used to disable the echo suppressors when an externally generated 2,000- to 2,250-Hz command tone conditioning signal of approximately 0.4-second duration is received. This allows for transmission of telegraph or data signals over the voice channel.

a. For the following analysis it is assumed that subscriber at station A is speaking and station B is listening. The voice signal from station A is received at the receiver echo suppressor at station B and produces a control signal output which is applied to the transmitter echo suppressor at station B. The control signal opens the transmit signal path in the echo suppressor and prevents the received station A voice signal from returning to station A. This results in a suppression of the echo at station A of more than 60 db.

b. Mode 2 operation occurs when one party is speaking and the other party interrupts. Partial echo suppression is achieved by inserting loss in the transmission paths. If the same amount of loss is inserted in each path, the echo suffers twice as much as the signal. Therefore, the echo becomes unnoticeable while both parties are speaking. Assume that the person at station A is speaking and the person at station B interrupts. When this occurs, the person's voice at station B overrides the control signal from the station B receiver echo suppressor and allows the station B voice to be transmitted through the transmitter echo

suppressor to station A. When both parties are speaking, fewer pads are electrically switched into the transmission path of all four echo suppressors, and each voice signal is attenuated by two of the loss pads (one transmit and one receive) while each speaker's echo signal is attenuated by all four loss pads. When one person stops speaking, the echo suppressors return to mode 1 operation.

c. The disabler unit has two modes of operation; guard and operate-hold. The disabler monitors both the transmit and receive voice paths. The guard circuit prevents the disabler from operating during speech transmission. This is accomplished by utilizing energy in the voice channel, which is outside of the conditioning band, to oppose any speech energy which falls into conditioning band. Upon receipt of the conditioning tone (2,000 to 2,250 Hz), the operate circuit causes the disabler to activate, and the hold circuit will keep the disabler in this status as long as the telegraph or data signals are present. Upon the absence of a signal for greater than 0.125 second, the disabler returns to the guard mode. When the disabler is activated, the outputs prevent the echo suppressors from switching in the loss pads or breaking the transmission path.

Section IV. ANTENNA CONTROL FUNCTION

2-68. General

The antenna control circuits function to position the AN/TSC-54 antenna at the selected satellite and attempt to keep the satellite within the antenna beamwidth by various tracking procedures so that communications can be supported. The satellite transmits a tracking beacon signal which is processed by the beacon demod and the resultant error signal is applied to the antenna positioning circuits. The beacon signal can be processed by either of the two comm demods in case of a beacon demod failure, and a communications signal can be utilized as a tracking signal, through one of the comm demods, to produce an error signal. All three demods provide both a synchronous detect signal, used in normal operation, and an envelope detect signal, used in the forced track mode of operation.

a. In the forced track mode of operation, it is possible to track on a communications signal with a high modulation index. Thus, if the satellite tracking beacon signal fails, it is still possible to track the satellite on the communications signal.

b. A bar scan mode of operation is provided for use during acquisition. In bar scan, the antenna sweeps a specific sector about a point where acquisition is expected. The sector size and sweep rate are variable.

c. A rate augment mode of operation is provided to relieve the operator of having to continuously rotate the handwheels when tracking in the manual mode. The rate augment signal is superimposed on the handwheel position command and both may be used simultaneously. If the handwheels are not rotated, the rate augment signal provides a constant rotational velocity to the instrument servomotor, which, in turn, drives the antenna.

d. A pencil beam mode of operation is used when manually tracking the satellite. In this mode, the sum signal bypasses the error modulation phase, thus, eliminating the insertion loss normally incurred in the modulating directional coupler.

e. A narrowband mode of operation is provided to improve the quality of a weak tracking signal or a signal containing extraneous noise. In this mode, the higher harmonic components of the signal are filtered out, the bandwidth is narrowed, and the amplitude of the error signal is increased.

f. A follow-up disable mode of operation is provided to allow the system to be prepared to transfer surveillance to a second satellite while continuing to track the first satellite. Essentially, the follow-up loop is disconnected from the antenna and a digital indicator is set to the coordinates of the new satellite. When phase lock is broken with the first satellite, the antenna is moved to the coordinates set in the digital indicator.

2-69. Functional Analysis of Antenna Control Circuits

(fig. FO 2-3)

The selection of which demodulator supplies the error signal to the antenna control subsystem is controlled by the position of receiver select switch S1. When receiver select switch S1 is set to BEACON, the synchronous detect signal and envelope detect signal are applied from the beacon demod through tandem connections and sections A and B of receiver select switch S1 to relay A66 (sheet 2). When receiver select switch S1 is in either of the COMM 1 or COMM 2 positions, the synchronous and envelope detect signals are applied from comm demod A3 or A5, to relay A66.

a. An agc signal, from the particular demodulator

providing the error signal, is applied through receiver select switch S1-E to SIGNAL STRENGTH meter M1. During manual operation, the meter provides a visual indication of antenna position with respect to the satellite.

b. The selected error signal from relay A66 is applied to pin D12-4 of dual low level switch A22 and to dc gain set module A29. The output of dc gain set module A29 is applied through servo operational amplifier A28 to pin D12-2 of dual low level switch A22 (180 degrees out-of-phase with the signal applied to pin D12-4). Dual low level switch A22 is activated by the 25 pulses-per-second signal applied from scan generator A20 through level shifters A26 and A34. Pulses from scan generator A20 are also applied to the ferrite scanner in the rf enclosure on the antenna mast, through four line drivers and associated impedance amplifiers. The pulses to dual low level switch A22 are delayed in scan generator A20, to compensate for the propagation delay of the ferrite scanner pulses. Elevation error signals are applied to dual low level switch A30, which is also activated by pulses from scan generator A20, through level shifters A35 and A27. Thus, azimuth and elevation error signals are synchronized with the modulation of the sum and error signals in the ferrite scanner.

c. The azimuth error signal from dual low-level switch S22 is applied through gain set No. 2 and servo operational amplifiers A25 and A16 (sheet 7) to normally-open contacts 1 and 3 of relay A13. In the bar scan mode, relay A13 is deenergized; however, it is energized in autotrack and the azimuth error signal is applied through the closed contacts of relay A23. Relay A23 and relay A151 (sheet 8) are energized when the AN/TSC-54 is in standby or when the antenna is being slewed. When either of these conditions exist, the output of relay driver A85 (sheet 3) is low and relays A23 and A151 are energized. In this condition, capacitor A38 (sheet 8) is shorted out through relay A151, and feedback to servo operational amplifier A25 is provided through capacitors A17, A26, and A155. The output of servo operational amplifier A25 is applied through relay A23 (sheet 7) to provide a stability loop by canceling the output of the amplifier.

d. The azimuth error signal from relay A23 is applied to normally-open contacts 3 and 6 of relay A22. When not in the standby mode, relay A22 is energized and the azimuth error signal is applied to summing network A24. When operating in the wideband mode, relay A36 is deenergized and the summing network passes the error signal to servo operational amplifier A25 sheet 8). The output of servo operational amplifier A25 is applied to pins 5 and 9 of resistor module A15 and to servo operational amplifier A51 through dc gain set A50.

e. When the antenna is slewed in azimuth, relay A49 is energized and the slew is applied to in 4 of dc gain set A50. However, during autotack the slew signal is not present, and the azimuth error signal is taken from the output of servo operational amplifier A51 and applied to parameter set A65. When the antenna is in the electric limit, it is backed out by the voltage applied through relay A64 (sheet 2) to pin 3 of parameter set A65.

f. The azimuth error signal is applied through servo operational amplifier A52 (sheet 8) two-operational amplifier A66. The output signal of operational amplifier A66 is applied through filter FL2B3 to dc power amplifier A1 (sheet 9). Dc power amplifier A1 supplies drive current to azimuth drive motor M1, through normally-open contacts of relay K1, to position the antenna in accordance with the azimuth error signal. Relay K1 is energized provided the system interlocks are closed and the system is not in standby.

g. Azimuth drive motor M1 is mechanically connected to tachometer generator G1. The output of the tachometer generator is applied through parameter set A65 (sheet 8) to the input of servo operational amplifier A52. This negative feedback is used as a control voltage to operational amplifier A66 to prevent excessive rive to dc power amplifier A18A1. The output of tachometer G1 is also applied to pin 27-4 of position memory parameter set A93.

h. During search and bar scan modes of operation, position memory is used to reposition the antenna to the point of initial signal detection. Before signal detection, the section of dual low level switch A103 controlled by level shifter A119, is open, and the other section controlled by level shifter A116, is closed. Thus, the output of tachometer G1 is grounded and operational modifier A105 is caged.

i. When a tracking signal is detected, the demodulator produces a satellite detect signal. For example, if beacon demod 1A3A4 (sheet 1) is being used, a ground level is provided at pin U of connector J6. This level is applied through section C of RECEIVER SELECT switch S1 to the satellite detect and phase lock logic circuits on the antenna control panel upper module board k23.

j. The satellite detect signal, from the beacon demod, is applied to relay driver A97 (fig. FO 2-6, sheet 4) and to section B of dual NAND gate A94. The output

of relay driver A97 is applied through lower module board A24 to illuminate SIGNAL DETECT indicator lamp DS1. The output of section B of dual NAND gate A94 goes high and enables section A of dual NAND gates A94 and A95. The low output of NAND gate A95 is applied through relay driver A98 to illuminate POSITION MEMORY indicator lamp DS2. Also, the low outputs of NAND gate A95 and section A of dual NAND gate A94 are inverted by dual NAND gate A96 and are applied to level shifters A63 and A116. The output of section A of dual MAND gate A94 is also applied to level shifter A115.

k. In this condition (*j* above) the section of dual low level switch A103 (pins 7 and 10, sheet 8) controlled by level shifter A116 is open, allowing the output of tachometer G1 (sheet 9) to be applied to the position memory circuit. The other half of dual low level switch A103 (pins 3, 4, and 9), which is controlled by level shifter A119, is closed, and operational amplifier A105 is uncaged. In addition, the section of dual low level switch A76 (pins 3, 4, and 9) controlled by level shifter A63 is open, applying the output of operational amplifier A105 to dc gain set A50. As a result, the output of tachometer G1 is integrated by servo operational amplifier A106. Amplifier A106 is a conventional dc operational amplifier, which operates as an integrator amplifier by virtue of the feedback through capacitor No. 2 module A118. The signal is then amplified by operational amplifier A105. The integrated, amplified position memory signal, when applied to servo operational amplifier A51, causes the antenna to return to the point where satellite detection was initially made.

l. If a phase lock condition is not accomplished within 4 seconds after initial detection of the satellite, the satellite detect signal and the position memory circuit is disabled, SIGNAL DETECT indicator lamp DS1 (fig. FO 2-6, sheet 4) extinguishes, and the antenna returns to the search mode. If phase lock is accomplished within 4 seconds, a phase lock command is produced by the demod. For example, when beacon demo 1A3A4 (sheet 1) is providing the error signal a +10 vdc level is provided at pin R of connector J6. This signal is applied through section D of RECEIVER SELECT switch S1 and the satellite detect and phase lock logic circuits, to illuminate PHASE LOCK indicator lamp DS3 (fig. FO 2-6, sheet 4) in the same manner as the satellite detect signal. Also, when phase lock occurs, the SIGNAL DETECT and POSITION MEMORY indicators extinguish.

m. The azimuth voltage feedback signal is taken from terminal E2 of dc power amplifier 18A1 (sheet 9). The signal is applied through resistor R1, filters FL1-1B and FL2A1, and dc gain set A130 (sheet 8), to operational amplifier A132. The output from amplifier A132 is applied through de gain set A145 and operation amplifier A147, to the azimuth channel through normally-closed contacts 1 and 3 of standby mode, the voltage feedback signal is applied to servo operational amplifier A25 (sheet 8) to prevent antenna drift and lock the antenna in a stable position.

n. When the AZIMUTH SLEW control is rotated, a ground level is applied through the normally-open contacts and upper module board A23 to energize relay A49. With relay A49 energized, the azimuth slew signal is applied through normally-open contacts 3 and 6 of relay A49 (sheet 8) to dc gain set A50. The azimuth slew signal originates at AZIMUTH SLEW potentiometers R1 and R2 (sheet 7). The signal is applied to servo operational amplifier A51 (sheet 8) through de gain set A50, to rotate the antenna in the cw or ccw direction depending upon the polarity of the slew signal.

o. When MANUAL pushbutton switch A5 (fig. FO 2-6, sheet 2) is depressed, a ground level is applied through tandem connections to pin 2 of NAND gate A40. NAND gates A39 and A40 are cross-connected to form a flip-flop. As a result, the output at pin 10 of NAND gate A39 goes low and is passed through relay driver A9 to energizes relay A64 (fig. FO 2-6, sheet 2). Consequently, the signal provided at pin 6 of relay A64 is applied to pin 3 of parameter set A65 (sheet 8). This signal, which is a function of either rate limit or servo limit, is inserted into the azimuth channel when these limits are entered.

p. When a rate limit (295 degrees cw or ccw) is entered, the wiper arm of deck F of azimuth limit switch S1 (fig. FO 2-6, sheet 1) closes between terminal C and NO. The ground level previously applied through filter FL2A4 to the coil of relay A77 (fig. FO 2-6, sheet 2) is removed, and relay A77 deenergizes. In this condition, a voltage level developed across resistors R1, R2, R5, and R6, of limit level set A92, is applied through contacts 1 and 3 of relay A77.

q. From relay A77, the voltage level is applied through contacts 6 and 3 of energized relay A64 to pin 3 of parameter set A65 (sheet 8). The antenna rotates cw or ccw to enter the 290-degree rate limit. The direction of rotation is determined by the polarity of the error signal at the output of servo operational amplifier A51. Regardless of the direction of rotation, current flows

through either diode CR3 or CR4 of quad diode A91 (fig. FO 2-6, sheet 2). Thus, the azimuth error signal is clamped below 12 volts in parameter set A65 (sheet 8) to limit the speed of antenna rotation after it passes the 295 degree point in either direction. The slew input remains enabled, and the antenna can be slewed in either direction, while in the 295- to 300- degree rate limit sector.

r. Between 300 degrees and 305 degrees, in either sector, the antenna is in the servo limit. In this sector, the antenna can be slewed in either direction, at the reduced rate speed, but only after overriding the servo limit stop. When the antenna rotates to the 300 degree point (either cw or ccw), the wiper arm of section H of azimuth limit switch S1 (fig. FO 2-6, sheet 1) closes between terminals C and NO. The ground level, which was previously applied through filter FL2C2 and the normalled-closed contacts of AZIMUTH SERVO LIMITS switch A12 to the coil of relay A78 (fig. FO 2-6, sheet 2) is removed. With the relay deenergized, a ground level is applied through contacts 7 and 9 to illuminate AZIMUTH SERVO LIMITS switch-indicator A12 (fig. FO 2-6, sheet 1).

s. A voltage level, developed across resistors R3 and R4 of limit level set module A92 (fig. FO 2-6, sheet 2), is applied through relay A90. The polarity of the level is determined by the condition of relay A90 (which is set when the antenna is in the ccw sector). The voltage at pin 3 of relay A90 is applied through contacts 3 and 1 of relay A78 and through contacts 6 and 3 of relay A64 to parameter set A65 (sheet 8). Thus, the antenna is automatically backed out of the servo limit. However, the back out function can be inhibited to allow the antenna to remain in the limit, by depressing AZIMUTH SERVO LIMITS switch A12 to cause relay A78 to deenergize and re move the servo limit back out voltage from parameter set A65. In this condition, the antenna can be slewed (at the reduced rate) in either direction. When AZIMUTH SERVO LIMITS switch A12 is released, the process is reversed and the antenna is backed out of the servo limit.

t. If the servo limit back out voltage is overridden and the antenna is rotated to 305 degrees, electrical control of the antenna is lost. This condition is incorporated to prevent damage to the antenna that could result from being driven into the mechanical stops. When the antenna reaches 305 degrees, the wiper arm of deck E of azimuth limit switch S1 (fig. FO 2-6, sheet 1) closes between terminals C and NO. With the limit switch in this condition, two actions take place:

(1) First, the interlock circuit is opened and lay A153 is deenergized. With relay A153 deenergized, a low level is present on pin 2 of AND gate A39 (fig. FO 2-6, sheet 3) causing flip-flop A39 and A40 to change state and deenergize relay A64 (fig. FO 2-6, sheet 2). In addition, the low input at pin 2 of NAND gate 39 is applied through relay driver A36 to energize relay K25 (fig. FO 2-6, sheet 4). Thus, the 28 vdc is removed from the panel indicators and all lamps remain extinguished.

(2) Second, with the wiper arm of deck E of azimuth limit switch S1 (sheet 1) closed between terminals C and NO, a ground level is provided connector J1-P of azimuth drive assembly A22. The ground level is applied through filter FL2A2 to normally-open contact C2 of AZIMUTH ELECTRIC LIMITS switch A13 causing it to illuminate. When switch A13 is held depressed, the azimuth electric limit signal round level is applied through contacts C2 and NO 2 to energize relay A67 (fig. FO 2-6, sheet 2). The azimuth electric limit signal also energizes relay A152.

u. With relay A152 energized, the output of servo operational amplifier A51 (sheet 8) is clamped to ground through contacts 4 and 7 relay A152. In this condition, the antenna is controlled by the voltage applied to parameter set A65 through contacts 1 and 3 of deenergized relay A64 (*t* (1) above). This voltage is applied to relay A64 through normally-open contacts 3 and of energized relay A67. The voltage applied to relay A67 is applied through contacts C1 and NO of AZIMUTH ELECTRIC LIMITS switch A13. The voltage at AZIMUTH ELECTRIC LIMITS switch A13 contacts is developed at azimuth limit level set potentiometer R8.

v. The polarity of the voltage across potentiometer R8 is determined by the condition of azimuth sense relay A90. When the antenna is the ccw sector, the C and NC contacts of deck of azimuth limit switch S1 (fig. FO 2-6, sheet 1) are closed. In this condition, a ground level is applied through pin S of connector J1 of azimuth drive assembly A22 and filter FL2A3 to energize relay A90 (fig. FO 2-6, sheet 2). With relay A90 energized, a negative voltage is developed cross potentiometer R8 and the antenna is driven in the cw direction when AZIMUTH ELECTRIC LIMITS switch A13 is depressed. Conversely, when the antenna is in the cw electric limit, the voltage across potentiometer R8 is positive. As a result, the antenna is driven in the ccw direction (or

backed out) when AZIMUTH ELECTRIC LIMITS switch A13 is depressed.

NOTE

It is also possible to enter the antenna into the electric limit by releasing the brake on the pedestal and rotating the antenna with the pedestal handcrank.

w. In case the tracking signal contains extraneous noise or is of low amplitude, causing unstable movement of the antenna, the narrowband mode can be used to improve the quality of the signal. The narrowband circuit is activated by depressing NARROWBAND switch A11 (fig. FO 2-6, sheet 4). When depressed, the switch lamp illuminates and a ground level is applied through normally-open contacts C1 and NO 1 to energize relays A35 through A37. Relay A35 is part of the elevation channel and performs the same function as relay A37 in the azimuth channel.

x. With relay A36 energized, a ground level is applied to pin 5 of summing network A24 (sheet 7) to ground resistor R8. When relay A37 (sheet 8) is energized, capacitors A17, A26, and A155 are connected in the servo operational amplifier A25 feedback loop in place of capacitor A38. Thus, the capacitance is increased from 7 μf to 21 μf and the higher harmonic components are filtered out, the bandwidth is narrowed, and the amplitude of the error signal is increased to reduce antenna jitter and instability.

y. The azimuth followup loop provides a positioning voltage to servo operational amplifier A25 when operating in any manual mode except slew. Also, the AZIMUTH handwheel and digital display are driven by the followup loop, except when the loop is disabled.

(1) The azimuth followup signal originates at resolver B1 in azimuth drive assembly A22 (sheet 5). Resolver B2 generates a voltage corresponding to the position of the antenna and the voltage phase is dependent on the reference voltage applied to rotor R2 and R4 of the resolver. The output from stator winding S1 through S4 is applied through filters FL3C1 through C4, and zero set resolver B2 to inputs S1 through S4 of azimuth followup resolver B3. During autotrack or forced track mode of operation, relay K3 (sheet 6) is deenergized.

(2) The azimuth followup resolver signal is routed from rotor winding R1 of resolver B3, through normally-closed contacts A2 and A3 of relay K3, normally-closed contacts B2 and B3 of relay K1, and relay K2 to azimuth followup power amplifier AR1, which drives azimuth followup drive motor B1.

(3) When azimuth followup brake L1 is released, the motor drives a mechanical linkage that positions the AZIMUTH digital position display. The followup loop is completed by mechanical linkage back to the rotor of azimuth followup resolver B1 (sheet 5), and the corresponding antenna position is indicated on the AZIMUTH digital display.

z. If it is desired to switch from a satellite being tracked to another satellite, disabling the followup loop allows the antenna to track the first satellite while the AN/TSC-54 is being prepared to track the second. When FOLLOWUP DISABLE switch S9 (fig. FO 2-6, sheet 4) is depressed, a ground level is applied through switch NO. 1 and C1 contacts to the inverter (section B) of dual NAND gate A136. The resultant high output of the inverter is applied to section A of dual NAND gate A134, enabling the gate. The output of the gate goes low and sets dual NAND gate (flip-flop) A135. The low output at pin 9 of flip-flop A135 is applied through relay driver A137 to illuminate the lamp in FOLLOWUP DISABLE switch A9 and to energize relay K2 (fig. FO 2-6, sheet 5).

aa. The low-level, following disable command, at pin 9 of flip-flop A135 (fig. FO 2-6, sheet 4) is also applied to relay drivers A33, A57, and A71. The resultant low output of relay driver A33 energizes azimuth followup clutch L2 (sheet 6) and engages the AZIMUTH handwheel. The low output of relay driver A71 energizes azimuth followup brake L1 to lock the followup drive motor and generator in place. In this condition, the AZIMUTH handwheel can drive the digital display to the azimuth intercept point of the second satellite. The low-level output of relay driver A71 (fig. FO 2-6, sheet 3) is also applied to section A of gate expander A58. As a result, a low-level is applied to energize azimuth followup resolver transfer relay K3 (fig. FO 2-6, sheet 5).

ab. When contact with the first satellite is broken, the phase lock signal at the input to NAND gate driver A107 (fig. FO 2-6, sheet 4) goes high. The high output of the NAND gate driver is applied to dual NAND gate A108 causing the output at pin 9 to go high and enable section A of dual NAND gate A136. The resultant low output at pin 9 of gate A136 is applied to pin 1 of NAND gate A29 (fig. FO 2-6, sheet 3), disabling the gate. The high output of NAND gate A29 is inverted by NAND gate A30, passed through NAND driver A31, and resets the flip-flop circuit consisting of A39 and A40, and flip-flops A53, A68, and A81. The high level output of dual NAND gate A108 (fig. FO 2-6, sheet 4), in addition to enabling

dual NAND gate A136, is also applied to relay driver A138. The resulting high output of the relay driver deenergizes relay A13.

NOTE

Depressing the MANUAL MODE CONTROL switch or rotating either SLEW control, disables NAND gate A29 with the same result.

ac. With relay K2 energized (*z* above), contacts B1 and B2 (sheet 6) make, and followup power amplifier AR1 is removed from the circuit. With relay K3 energized (*aa* above), a signal proportional to the position of the azimuth followup resolver (representing the azimuth intercept point of the second satellite) is applied to the normally-closed contacts of relay A4.

NOTE

Relay A4 is only energized for operating in the program mode.

ad. The followup resolver error signal is applied to servo operational amplifier A2 through gain set No. 2. The output of servo operational amplifier A2 is applied to one-half of dual low-level switch A10 and to gain set No. 2. Amplifier A8 inverts the signal from gain set No. 2 and applies it to the other half of dual low-level switch A10. Thus, the two resolver error signals are applied to the two halves of dual low-level switch A10, 180 degrees out-of- phase. Low-level switch A10 is operated by signals from shaping circuit A1.

ae. The 120 vac, 400 Hz signals at pins A and B of connector W8P1 is applied through circuit breaker CB1 (sheet 2), transformer T1, and resistors R2 and R11 to shaping circuit A1 (sheet 6). The 400 Hz sine wave is converted to a 400-Hz square wave by shaping circuit A1 and complementing pulses are applied to dual low-level switches A10 and A11. Thus, the resolver error signal is synchronized with the 400 Hz reference signal, applied to the azimuth resolvers and synchros, to assure proper direction of rotation of the antenna azimuth drive motor.

af. The signals from dual low-level switch A10 are combined at gain set No. 2A16 and amplified by servo operational amplifier A14. The output of amplifier A14 is applied to dc gain set A7 (sheet 7) through pin 39 of connector W1P1. From dc gain set A7, the signal is applied through servo operational amplifier A8, to normally-closed contacts 6 and 3 of deenergized relay A13 (*ab* above). With relay A13 deenergized, the resolver error signal is applied to the azimuth drive motor to position the antenna to the intercept point of the new satellite.

ag. The output of synchro B1 (sheet 5) is proportional to the antenna azimuth position. This signal is applied through zero set control synchro B1 (sheet 4) to azimuth synchro receiver . Zero set synchro B1 is adjusted to position indicator to 0 degree when the antenna is pointed at true north. Due to the difference in magnetic north and true north, and the difficulty that is encountered in aligning the antenna on a true north-south line, the zero set synchro is rotated to insert a correction factor to the AZIMUTH digital readout.

ah. Azimuth cable wrap synchro B1 supplies signal to the AZIMUTH CABLE WRAP indicator, which is the short pointer in the ZIMUTH position indicator. The green band the indicator dial shows the direction and amount of cable wrap. Three hundred degrees of travel on either side of the stow position is allowed before the pointer leaves the green band.

ai. Scan generator A20 (sheet 2) produces signals for synchronizing the tracking error signal with the modulation taking place in the rite scanner. The 400-Hz reference voltage from pins A and B of connector W8J3 is applied rough 400 CPS REF circuit breaker CB8 and transformer T2 to zener diode CR1. The resulting half cycle of the sine wave is formed into a square wave by the pulse shaping network composed of the invertor (section A) of NAND gate and capacitor C6.

aj. The 400-Hz square wave is counted down 100 cps by the divide-by-4 counter circuit composed of flip-flops A2 and A3. The 100-Hz pulse train triggers a 3-stage ring counter circuit composed of flip-flops A4, A5, and A6.

ak. If all three stages of the ring counter (*aj* above) are initially set, section B of NAND gate 1 is enabled and a low level is applied to the set control input of flip-flop A4. This low level is also applied to inverter section D of NAND gate A15 rich produces the first positive-going scan pulse. The low input of section B and NAND gate A1 is also inverted by inverter section A and NAND gate A12 and is applied to the clear control input of flip-flop A4. Thus, the first negative-going, 100-Hz trigger pulse from flip-flop A3 triggers (resets) flip-flop A4 while the last two stages remain set.

al. In this condition (*ak* above) section B of AND gate A1 is disabled, the control inputs to the first stage are reversed, and the first scan pulse is terminated. This 10-ms pulse is passed rough line driver A44 and impedance amplifier A45 and becomes ferrite scan pulse 1 shown on the functional diagram. With flip-flop A4 reset, a low level is applied to pin 2 of inverter section C of NAND gate A15 which is subsequently inverted to produce ferrite scan pulse 2.

am. The second trigger pulse sets flip-flop A4, resets flip-flop A4, resets flip-flop A5, and the last stage remains set. As a result, ferrite scan pulse 2 is terminated and scan pulse 3 is developed at pin 11 of inverter section B of NAND gate A15. This process continues as pulses 3 and 4 are produced and the cycle is continuously repeated. If initially, all stages of the ring counter are not set, section B of NAND gate A1 is disabled. The resultant high output of the gate holds the set input of the first stage enabled until all stages are set and then the counter starts to count normally.

an. The false output at pin 10 of flip-flop A3 is applied to pin 2 of the inverter module A14. The signal is inverted twice in module A14 and the low output is applied to a delay network consisting of section A of NAND gates A11 and A10. When the low level terminates, the inputs at pins 4 and 13 of NAND-2 gate A10 are high and the gate is enabled and remains enabled until capacitor C3 discharges. Thus, the trailing edge of the negative output is delayed by an amount proportional to the value (selected at test) of capacitor C3.

ao. The process is repeated by the delay network consisting of section B of both NAND gates A11 and A10. The positive-going edge of the pulse is thus delayed in amount proportional to the value of capacitor C4, which is also selected at test. The pulse is inverted by section B of NAND gate A12 and the resultant negative-going trailing edge triggers a 4-stage ring counter circuit consisting of flip-flops A9, A8, A7, and A13. This trigger resets the first stage of the 4-stage ring counter. The resultant low level at the true output (pin 14) of the first stage is applied to inverter section D of NAND gate A16. The positive output at pin 5 is applied through level shifter A26 to dual low level switch A22. In this manner, this half of dual low level switch A22 is operated simultaneously with the reception of ferrite scan pulse 1 at the ferrite scanner. The remaining three delayed pulses are generated in a similar manner for application to the phase demodulator circuit.

2-70. General Analysis of Operational Modes

(fig. FO 2-6, sheets 3 and 4)

Paragraphs 2-70 through 2-73 contain descriptions of the prestandby interlock, standby, manual, and acquisition modes of operation. Tables of logic outputs of applicable gates are included in each paragraph for a quick reference to circuit conditions for the different operational modes. The referenced gates are illustrated in figure FO 2-6, sheets 3 and 4. The outputs of the logic gates, for the three manual and four acquisition modes, are provided below.

	Manual			Acquisition			
Gate	**Handwheel**	**Rate augment**	**Slewing**	**Bar scan**	**Autotrack**	**Satellite detect**	**Phase lock**
A9	0	0	0	0	0	0	0
A10	0	0	0	0	0	0	0
A18	0	0	0	0	0	1	1
A36	1	1	1	1	1	1	1
A33	0	0	0	0	0	1	1
A43	1	1	1	1	1	1	1
A46	1	0	1	1	1	1	1
A57	0	1	1	0	0	1	1
A38							
A&B	0	0	1	1	1	1	1
A71	0	1	1	0	0	1	1
A72	1	1	1	0	0	1	1
A84	1	1	1	1	1	1	1
A85	1	1	0	1	1	0	1
A8-1A	1	1	1	1	1	0	0
A96-A	0	0	0	0	0	1	0
A96-B	0	0	0	0	0	1	1
A97	1	1	1	1	1	0	0
A98	1	1	1	1	1	0	1
A110	I	1	1	1	1	1	0
A111	1	1	1	1	1	1	0
A112	1	1	1	1	0	0	1
A173	1	1	1	1	1	1	1
A137	1	1	1	1	1	1	1
A138	1	1	1	1	1	1	0

2-71. Analysis of Prestandby Interlock Mode of Operation
(fig. FO 2-6)

a. The interlock circuit basically consists of a series of switches and relay contacts. When an interlock is open, the system is in the prestandby mode and power is removed from the antenna drive motors. When all interlocks are closed, relay A153 (sheet 1) is energized and the system is automatically placed in standby. The ground level that energizes relay A153 is applied through contacts C and NC on deck C of elevation limit switch S1, provided the antenna electrical limits are not exceeded in elevation. The ground level is applied through normally-open contacts of relays K5, K4, and K2 in servo amplifier A3.

b. Relay K5 is energized provided power is applied to elevation drive motor B1 field windings F1 and F2 (fig. FO 2-3, sheet 9). This power is received at pin 6 of cables W2 and W3 in primary power distribution panel A14 (fig. FO 2-7, sheet 2) and is applied through circuit breaker A14 (fig. FO 2-7, sheet 2) and is applied through circuit breaker CB8 to a diode bridge circuit consisting of diodes CR4 through CR7 on servo amplifier A3. The full-wave rectified power at the bridge output causes current to flow through the motor field winding and the coil of relay K5, which are in series. Thus, when field current is interrupted, the relay deenergizes and the interlock circuit is open.

c. Relay K4 (sheet 6) is energized as long as drive motor B1 overload sensor switch, in the elevation head assembly, is closed. This switch is closed until an overload is placed on the motor. Relay K2 (fig. FO 2-7, sheet 2) is energized as long as EL DRIVE circuit breaker CB12, on primary power distribution panel A14, is closed and prime power contractor relay K4 is energized. When these conditions exist, ac power is applied to the elevation servo amplifier.

d. From servo amplifier A3, the ground level is applied through mast fold interlock switch S1, which is closed when the antenna mast is fully extended upward. The level is applied through azimuth electric limit switch S1 and relays K5, K4, and K2, in servo amplifier A17, in the same manner as through the elevation limit switch S1 and servo amplifier A3 (*b* above). When the azimuth stow pin is removed from the stow hole and inserted in the storage or operate hole, azimuth stow interlock switch S1 is closed and the ground level is applied to MOUNT SAFE toggle switch S2.

e. The ground level is applied through elevation cable wrap A5 to microswitches S1 and S2 located on each side of the antenna's elevation axis. If the antenna is operated in elevation while the work platform guard rails are in place, actuating plates on the guard rails S1 and S2 to open; and the antenna is placed in a mount safe condition. When switches S1 and S2 are closed, the ground level is applied to MOUNT SAFE toggle switch S2.

f. Provided MOUNT SAFE toggle switch S2 is closed, the ground level is applied to four power supply relays on lower module board A24. Provided these power supplies are operating, power is applied to energize the respective relay coils sheet 5). In this condition, the ground level is applied through the series-connected contacts of relays A60, A61, A58, A59 and 400 CPS reference interlock (sheet 1) to energize relay A153.

g. Flip-flops A39 and A40 (sheet 3) are normally in the set condition due to the action of capacitor C5. This capacitor holds the output of lip-flop A40 low and applies the low to an input of flip-flop A39 causing that output to go high and therefore, assume the set state. In this condition, the low output from inverter section A of dual NAND gate A28 will have no effect. However, when operating in the manual mode, flip-flops A39 and A40 are in the reset state and he low output from section A of NAND gate A28, as a result of an interlock opening, sets the lip-flop and returns the antenna control system to prestandby. If an interlock is open, a low level is applied to flip-flop A39, and the manual mode cannot be entered because flip-flops A39 and A40 cannot be reset.

h. With flip-flops A39 and A40 set, the high at pin 10 is applied to relay driver A10. Relay driver A10 is enabled, provided the antenna control system is not in the followup disable node, and the resultant low level output is applied as follows:

(1) First, relay A63 (sheet 5) is deenergized, which causes relays A17K3 and A3 (fig. FO 2-3, sheet 9) to deenergize. As a result of this action, brake excitation is removed and the antenna brakes are applied.

(2) Second, relay A22 (fig. FO 2-3, sheet 6) is deenergized so that the output from operational amplifier A147 (fig. FO 2-3, sheet 8) is fed back to servo amplifier A25.

i. When all interlocks are closed, relay A153 is energized and a high enabling signal is applied to NAND gate A39 of flip-flop A39 and A40. The high level also deenergizes relay K25 and illuminates the panel indication lamps. In this condition, the system is in the standby mode and flip-flop A39 and A40 can be reset by a low manual command (at pin 2 of NAND gate A40.)

j. Applicable logic outputs for the prestandby mode of operation are provided below.

2-72. Analysis of Standby Mode of Operation
(fig. FO 2-6)

a. The antenna control system automatically transfers from prestandby, provided the

Gate	Logical output	Function initiated	Display or end result observed
A36	0	Indicator inhibit relay is energized.....	MODE CONTROL, BEACON RECEIVER, and FOLLOWUP DISABLE indicators are prevented from illuminating.
A9	1	Rate and servo limit relay A64 is deenergized	None.
A10	1	*a*. (B1-10) output deenergizes standby relay A6, that deenergizes brake solenoid relays. *b*. (A23-8) output deenergizes standby feedback relay A22.	*a*. Antenna brakes applied. Power distribution panel ANTENNA STATUS indicators are illuminated as applicable. *b*. Power amplifier output is applied back to position loop amplifier input.
A43	0	None, because indicator power return is removed by indicator inhibit relay being energized.	STANDBY indicator is extinguished.
A33	1	Handwheel clutch solenoids are deenergized.	Handwheel positioning is disabled.
A18	1	None	MANUAL indicator is extinguished.
A46	1	Rate augment relay K1 is deenergized.	Rate augment is disabled and RATE AUGMENT indicator is extinguished.
A38	1	Followup resolver transfer relays K3 and K3 are deenergized.	Resolver output is connected to followup loop.
A137	1	Followup relays K2 and K2 are deenergized.	Resolver output is connected to followup loop.
A71	1	Azimuth followup brake L1 solenoid is deenergized.	Followup loop is complete, permitting followup to respond to antenna positioning.
A57	1	Elevation followup brake L1 solenoid is deenergized.	Followup loop is complete, permitting followup to respond to antenna positioning.
A72	1	Bar scan relay A14 is deenergized.	Scan generator input to scan amplifier is disabled and BAR SCAN indicator is extinguished.
A84	1	Program relay A4 is deenergized.	Program input to scan amplifier is disabled. PROGRAM indicator is extinguished.
A85	1	Position amplifier caging relays A23 and A151 are deenergized.	Position amplifier is uncaged to permit response to standby feedback voltage.
A97	1	None	SIGNAL DETECT indicator is extinguished.
A98	1	None	POSITION MEMORY indicator is extinguished.
A96A	0	Dual low level switch A76 contacts are closed.	Output of position memory is shunted to ground.
A96B	0	One-half of dual low level switch A103 (pins 7 and 10) is closed.	Data from tachs is shunted to ground.
A94	1	One-half of dual low level switch A103 (pins 3, 4, and 9) is open.	Position memory amplifier output is fed back.
A111	1	None	PHASE LOCK indicator is extinguished.
A110	1	None	AUTOTRACK indicator is extinguished.
A112	1	None	ACQUISITION indicator is extinguished.
A138	1	Track relay A13 is deenergized.	Output of scan summing amplifier is applied to position amplifier.
A173	1	None	FORCED TRACK indicator is extinguished.

interlock circuit is closed, after the initial application of power. When all interlocks are closed, interlock relay A153 (sheet 1) is energized and the inverter of dual NAND gate A28 produces a high output. This high level enables flip-flops A39 and A40 (sheet 3) so that a negative pulse, applied to the A40 input, will reset the stage. The high level from dual NAND gate A28 also deenergizes indicator inhibit relay K25 (sheet 4) to illuminate the panel indicators. Thus, the STANDBY indicator is illuminated by the lowlevel output of relay driver A43 (sheet 3).

b. When the system is operating in the manual mode or any other operational mode, the system can be returned to standby by depressing STANDBY pushbutton switch S1. This action applies a ground level to pin 3 of flip-flop A39 causing flip-flops A39 and A40 to return to the set state.

2-73. Analysis of Manual Mode of Operation

(fig. FO 2-6)

a. When the system is in standby, the manual mode can be achieved by depressing MANUAL pushbutton switch A5 (sheet 3). This action applies a ground level to pin 2 of flip-flop A39 causing the flip-flop A39 and A40 to reset. The ground level is also applied to NAND gate A9, which produces a trigger pulse to reset mode control flip-flops A53, A68, and A81. With flip-flop A39 and A40 reset, STANDBY indicator A1 (sheet 4) extinguished and standby feedback relay A22 is energized because of the low output of relay driver A10 (sheet 3). With relay A22 energized, the error signal is applied to servo amplifier A25 (fig. FO 2-3, sheet 8). The low output of relay driver A10 also energizes relay A63 (sheet 5) and as a result, the azimuth and elevation brakes are released.

b. In the manual mode, the output of relay driver A9 goes low and energizes rate and servo limit relay A64 (sheet 2) to provide back out voltage in servo limits. The output of relay driver A33 also goes low and energizes the followup clutches to enable the handwheels. The MANUAL indicator illuminates because of the low output of relay driver A18.

c. Applicable logic outputs for manual mode (using handwheels) are provided below.

Gate	Logical output	Function initiated	Display or end result observed
A36	1	Indicator inhibit relay K25 is deenergized.	MODE CONTROL, FOLLOWUP DISABLE, and BEACON RECEIVER indicators are enabled to function according to operation.
A9	0	Rate and servo limit relay A64 is energized to connect servo limit backout voltage when servo limit is exceeded.	SERVO indicator illuminates when limits are exceeded. Antenna backs out of limit.
A10	0	Not standby relay A6 is energized; antenna brakes solenoid control is energized. Standby feedback relay A22 energized.	Antenna brakes are released. AZ BRAKE and EL BRAKE indicators extinguished. Followup loop is applied to position loop; antenna is positioned according to error signal.
A43	1	STANDBY indicator inhibited	STANDBY indicator is extinguished.
A33	0	Handwheel clutch solenoids are energized.	Handwheel positioning is enabled.
A18	0	MANUAL indicator enabled.	MANUAL indicator is illuminated.
A46	1	Rate augment relay K3 is de-RATE AUGMENT indicator is inhibited.	MANUAL indicator is illuminated. RATE AUGMENT indicator is extinguished.
A38-A A38-B	0	Followup resolver transfer relay K3 is energized.	Resolver output is connected to position loop amplifier via scanning amplifier.
A137	1	Followup relays K2 are de-energized	Followup amplifier input is made available for rate augment or resolver output.
A71	0	Azimuth followup brake L1 solenoid is energized.	Positioning of resolver rotor by follow-loop is disabled.
A57	0	Elevation followup brake L1 solenoid is energized.	Positioning of resolver rotor by followup loop is disabled.
A72	1	Bar scan relay A14 is energized. BAR SCAN indicator is inhibited.	Scan input is removed from position loop amplifier input. BAR SCAN indicator is extinguished.

Gate	Logical output	Function initiated	Display or end result observed
A84	1	Program relay A4 is de-energized. PROGRAM indicator is inhibited.	Program is removed from error phase demodulator input. PROGRAM indicator is extinguished.
A85	1	Position amplifier caging relays A23 and A151 are de-energized.	Position amplifier responds to error signal or standby feedback voltage.
A97	1	SIGNAL DETECT indicator. is inhibited.	SIGNAL DETECT indicator is extinguished
A98	1	POSITION MEMORY indicator is inhibited.	POSITION MEMORY indicator is extinguished.
A96A	0	Dual low-level switch A76 contacts are closed.	Output of position memory is shunted to ground.
A96B	0	One-half of dual low-level switch A103 (pins 7 and 10) are closed.	Data from tachs is shunted to ground.
A94	1	One-half of dual low-level switch A103 (pins 3, 4, and 9) are open.	Position memory amplifier output is fed back (amplifier is caged).
A111	1	PHASE LOCK indicator is inhibited.	PHASE LOCK indicator is extinguished.
A110	1	AUTOTRACK indicator is inhibited.	AUTOTRACK indicator is extinguished.
A112	1	ACQUISITION indicator is inhibited.	ACQUISITION indicator is extinguished.
A138	1	Track relay A13 is de-energized.	Output of scan summing amplifier is applied to position amplifier instead of beacon receiver error signal.
A173	1	FORCED TRACK indicator is inhibited.	FORCED TRACK indicator is extinguished.

d. When RATE AUGMENT switch A7 (sheet 3) is depressed, a ground level is applied to NAND gate A29 and to flip-flop A53. The flip-flop assumes the set condition and applies a high, enabling input to NAND gate A34. The resultant low output of NAND gate A34 is applied to relay driver A18, relay driver A46, NAND gate A55, and NAND gate A83.

e. The low level applied to NAND gate A55 causes the output to go high and enable relay driver A71. The resultant high output of relay driver A71 deenergizes azimuth followup brake L1 (fig. FO 2-3, sheet 6). Simularly, elevation followup brake L1 is deenergized through NAND gate A83 and relay driver A57.

f. The low input to relay driver A46 (sheet 3) produces a low-level output, which causes RATE AUGMENT indicator A7 (sheet 4) to illuminate and both rate augment relays (sheet 5) to energize. In this condition, the level from azimuth POSITION RATE potentiometer R3 (fig. FO 2-3, sheet 6), is applied to the azimuth followup circuit. The polarity and amplitude of the signal is dependent on the position of the potentiometer.

g. The rate augment signal is applied through winding F2 and F1 of azimuth followup generator B2 and chopper G1. Chopper G1 operates at 400 Hz and the resultant pulsating signal is applied through part of potentiometer R2 and the normally-open contacts of energized relay K1 to azimuth followup power amplifier AR1. Thus, with the followup brake released, the output of rate augment POSITION RATE potentiometer R3 drives the azimuth followup resolver at a constant rate.

h. The differences between rate augment logic and handwheel positioning logic are provided below.

Gate	Logical output	Function initiated	Display or end result observed
A46	0	Rate augment relay K1 is energized. RATE AUGMENT indicator is enabled.	Output of rate augment potentiometers is applied to followup loop. RATE AUGMENT indicator is illuminated.
A71	1	Azimuth followup brake L1 is deenergized.	Gear train is locked. Antenna moves according to rate augment potentiometer output.
A57	1	Elevation followup brake L1 is deenergized.	Gear train is locked. Antenna moves according to rate augment potentiometer output.

i. Slewing the antenna is performed as described in paragraph 2-69. The differences between slew logic and handwheel positioning logic are provided below.

j. The bar scan mode of operation is normally used to effect acquisition. Satellite acquisition is a combination of this mode of manual operation and autotrack, satellite detect (signal detect), and phase lock. In bar scan, the antenna is made to sweep a specific sector about a point where acquisition is expected. The size and shape of the sector is constantly adjustable between 0 and 5 degrees in azimuth and elevation. The antenna sweeps in azimuth at a rate that is variable between 0.0 and 1.0 degree per second. With each sweep in azimuth, the antenna steps up one increment in elevation until the sector is covered, at which time the antenna sweeps back down. The elevation increment, or height of step, is variable between 0.0 and 1.0 degree. Paragraph 2-74 describes the function of bar scan as part of acquisition.

2-74. Analysis of Acquisition
(fig. FO 2-6)

a. When BAR SCAN switch S6 (sheet 3) is depressed, a ground level is applied to NAND gate A29 and dual NAND (flip-flop) A68. As a result, all mode control flip-flops are reset except A68, which is set. The output at pin 10 ff A68 goes high and enables NAND A69 to produce a low output. This low level is passed through relay driver A72 to perform three actions. First, relays A14 and A48 are energized.
Second, BAR SCAN indicator A6 (sheet 4) illuminates and, third, relay A74 (sheet 5) is energized. As a result, the bar scan control potentiometers R5 through R8 (sheet 7) and bar scan generators are connected to the position loop.

b. AZ SECTOR potentiometer R5 (fig. FO 2-3, sheet 7) sets the width-between 1 and 5 degrees, of the azimuth sweep angle. AZ RATE potentiometer R7 is used to determine the speed at which the antenna scans within the sector. The rate is variable between 0.0 degree per second and 1.0 degree per second. These two controls combine to establish the characteristics of the sawtooth-shaped, azimuth scan signal.

c. The network of AZ RATE potentiometer R7, resistor R12, and capacitor A46 determine the frequency of the oscillator circuit composed of servo operational amplifier A36 and dc gain set A38. The amplitude of the sawtooth output of servo operational amplifier A36 is established by the level applied through AZ SECTOR potentiometer R5 to dc gain set A38. This sawtooth waveform is the azimuth scan output, which is applied to the azimuth position loop through normally-open contacts of energized relay A14. The positive-going excursion of the sawtooth drives the antenna ccw and the negative-going excursion drives it cw. The greater the peak-to-peak amplitude, the longer the azimuth switch angle.

d. The sawtooth signal is also taken from pin 3 of dc gain set A38 and applied to operational amplifier A37.

Gate	Logical output	Function initiated	Display or end result observed
A38A A38B	1	Followup resolver transfer relay K3 is deenergized.	Resolver output is applied to followup loop.
A71	1	Azimuth followup brake L1 solenoid is deenergized.	Azimuth followup brakes are released.
A57	1	Elevation followup brake L1 solenoid is deenergized.	Elevation followup brakes are released.
A85	0	Position amplifier caging relays A23 and A151 are energized.	Position amplifier is caged (not affected by error voltage).

The output of A37 is 180 degrees out-of-phase with the azimuth scan signal from amplifier A36 and is limited by diodes CR9 and CR10. When the output of operation amplifier A37 starts to go low, the output across a differentiator network composed of capacitor C1 and resistor R6, triggers flip-flop A40 to the reset state. One hundred and sixty milliseconds after being triggered, the output at pin 10 of variable time delay A47 goes low and sets flip-flop A40. When the output of operational amplifier A37 starts to go high, the output of inverter NAND gate A39 starts to go low. As a result, the output across the differentiator network consisting of capacitor C2 and resistor R5, triggers flip-flop A40 to the reset condition for another 160 milliseconds. Thus, each time the antenna scan signal changes direction, flip-flop A40 becomes set and allows the contacts of dual low-level switch A49 to open for 160 milliseconds. This open condition is applied to the elevation scan generator to synchronize the circuits.

e. EL INCREMENT potentiometer R8 is used to select the height of the step or increment that the antenna will change in elevation for each sweep in azimuth. This increment is variable between 0.0 and 1.0 degree. EL SECTOR potentiometer R6 sets the height (between 1 and 5 degrees) of the elevation scan angle. These two potentiometers combine to establish the characteristics of the step-function or elevation scan signal.

f. During the 160 milliseconds that the contacts of dual low-level switch A49 are open (*d* above), the oscillator circuit composed of servo operational amplifier A52 and capacitor NO. 2 A73 is allowed to integrate. The output of the amplifier builds up to a level proportional to the setting of EL INCREMENT potentiometer R8 (*e* above). When the antenna completes sweeping in the original direction, dual low-level switch A49 closes and the output of servo operational amplifier A52 increases another increment in elevation and the antenna sweeps in the opposite direction.

g. In the bar scan mode of operation, relay A47 is energized and feedback is provided for the oscillator (*f* above). The output of the oscillator is also applied to dc gain set A41. Outputs of dc gain set A41 are applied to operational amplifier A42 and to EL SECTOR potentiometer R6. When the output of servo operational amplifier A52 reaches a predetermined level, operational amplifier A42 saturates and the output goes negative. This negative level is applied through diode CR36 to the intersection of EL INCREMENT and EL SECTOR potentiometers R8 and R6. This level is applied through the wiper arm of EL INCREMENT potentiometer R8 to the input of servo operational amplifier A52.

h. As the output of servo operational amplifier A52 continues to rise, the output at pin 10 dc gain set A41 also increases. This increased output is applied through the wiper arm of EL SECTOR potentiometer R6 and opposes the output of operational amplifier A42, at the intersection of the two potentiometers. When the signal at pin 10 overcomes the level from operational amplifier A42, the output of servo operational amplifier A52 stops increasing. At this point, the circuit reverses operation and produces a step function down to the original elevation position and the cycle is repeated until the satellite is acquired. The step-function elevation scan signal is applied through normally-open contacts of energized relay A14 to the elevation position loop.

i. Each time the elevation scan signal changes amplitude, a pulse (of corresponding polarity) is applied to servo operational amplifier A57. The amplifier produces a pulse of corresponding polarity, which is applied through the normally-open contacts of energized relay A48 (fig. FO 2-3, sheet 8) to relay A44. Relay A44 is deenergized, except when slewing, and the elevation feed forward signal is applied to servo operational amplifier A46, through dc gain set A47. This signal is applied to the power amplifier A4 (fig. FO 2-3, sheet 9) to start driving the elevation drive motor in the proper direction.

j. Applicable logic outputs for bar scan are provided below.

k. When ACQUISITION/AUTOTRACK pushbutton switch A3 (sheet 4) is depressed, a ground level is applied to set flip-flops A119 and A120. The resultant

Gate	Logical output	Function initiated	Display or end result observed
A38	1	Followup resolver transfer relay is deenergized.	Resolver output is applied to followup loop.
A72	0	Bar scan relay A14 is energized. BAR SCAN indicator is enabled.	Scan generator output is applied to position loop; BAR SCAN indicator is illuminated.

high output at pin 10 of flip-flop A119 is applied as an enable signal to four NAND gates. Section A of dual NAND gate A94 is enabled in preparation for receiving a satellite detect signal. NAND gate A95 is enabled to receive a phase lock command, and section A of dual NAND gate A108 is prepared to receive a pencil beam command. Section A of dual NAND gate A109 is enabled and produces a low level at the output, which is applied through relay driver A112 to illuminate ACQUISITION/AUTOTRACK indicator lamp A3. Applicable logic outputs for the acquisition mode are provided below.

Gate	Logical output	Function initiated	Display or end result observed
A38A A38B	1	Followup resolver transfer relay K3 is deenergized.	Resolver output is applied to followup loop.
A72	0	Bar scan relay A14 is energized. BAR SCAN indicator is enabled.	Scan generator output is applied to position loop; BAR SCAN indicator is illuminated.
A112	0	ACQUISITION indicator is.	ACQUISITION indicator is illuminated

l. When a satellite detect command is received, a low level signal is applied to relay driver A97 which, in turn, illuminates SIGNAL DETECT indicator lamp DS1. The low level satellite detect signal is also applied to section B of dual NAND gate A94. Tye output at pin 10 goes high and enables NAND gate A95 and dual NAND gate A94A. The outputs of these two gates go low and cause POSITION MEMORY indicator lamp DS2 to illuminate and the position memory circuit returns the antenna to the point of signal detection.

m. Applicable logic outputs for the acquisition function, including bar scan, autotrack, and satellite detect, are provided below.

n. When the phase lock command is received, the system begins autotracking and a low level is applied to NAND gate driver A107. The lowlevel output of driver A107 disables NAND gate A95, which disables the position memory circuit and extinguishes POSITION MEMORY

Gate	Logical output	Function initiated	Display or end result observed
A33	1	Handwheel clutch solenoids are deenergized.	Handwheel positioning is disabled.
A18	1	MANUAL indicator is inhibited.	MANUAL indicator is extinguished.
A38A A38B	1	Followup resolver transfer relay K3 is deenergized.	Resolver output is applied to followup loop.
A71	1	Azimuth followup brake L1 solenoid is deenergized.	Azimuth followup brakes are released, allowing followup to provide digital readout of antenna position.
A57	1	Elevation followup brake L1 solenoid is deenergized.	Elevation followup brakes are released, allowing followup to provide digital readout of antenna position.
A85	0	Position amplifier caging relays A23 and A151 are energized.	Position amplifier is caged, output does not affect position memory input to tach.
A97	0	SIGNAL DETECT indicator is enabled.	SIGNAL DETECT indicator is illuminated.
A98	0	POSITION MEMORY indicator is enabled.	POSITION MEMORY indicator is illuminated.
A96A	1	Dual low level switch A76 contacts are opened.	Output of position memory circuit is applied to tach loop.
A96B	1	One-half of dual low-level switch A103 (pins 7 and 10)	Tach output is applied to position memory circuit.
A94A	0	One-half of dual low level switch A103 (pins 3, 4, and 9) is closed.	Position memory caging is removed.
A112	0	ACQUISITION indicator is enabled.	ACQUISITION indicator is illuminated.

indicator lamp DS2. The low output is also applied through relay driver A111 to energize phase lock relay A68 and cause PHASE LOCK indicator lamp DS3 to illuminate.

o. The low output of NAND gate driver A107 is inverted by the inverter section of dual NAND gate A108 and the resultant low output causes relay A13 to energize (to apply the tracking error signal to the position amplifier) and AUTOTRACK indicator lamp A3 to illuminate. In addition, the low output of NAND gate driver A107 disables dual NAND gate A109, which in turn, extinguishes ACQUISITION indicator lamp A3.

p. Applicable logic outputs for autotrack are provided below.

q. When FORCED TRACK pushbutton switch A4 is depressed, a ground level is applied to set flip-flop A121. The high output at pin 10 of flip-flop A121 enables section B of dual NAND gate A109, which produces a low-level output. This low level is applied through NAND gate driver A122 and relay driver A123 to energize relay A66 and cause FORCED TRACK indicator A4 to illuminate. With relay A66 energized, the envelope detect signal from the beacon demod (or comm demod) is applied to the antenna control system.

r. The low-level output of dual NAND gate A109 also disables relay driver A138 and energizes relay A13. With relay A13 energized, the tracking error signal is applied to the position loop amplifier circuit. The low-level output at pin 10 of dual NAND gate A109 becomes the forced track inhibit signal and disables NAND gates A42, A34, A69, and A82. With the gates disabled, all antenna positioning capabilities, except slewing and beacon tracking, are inhibited.

s. When PENCIL BEAM pushbutton A8 is depressed, the PENCIL BEAM indicator illuminates because of the ground potential applied through contacts C2 and No. 2. This ground level is also applied through contacts C3 and No. 3 to waveguide switch S13, which applies the received satellite signal direct to the parametric amplifier with no error modulation.

t. In addition, when the PENCIL BEAM pushbutton switch is depressed, a ground is applied to pin 3 of dual NAND gate A108. The resultant high output at pin 9 of NAND gate A108. The resultant high output at pin 9 of NAND gate A108 is applied to relay driver A138 and relay A13 is deenergized. In this condition, the output of servo operational amplifier A8 (fig. FO 2-3, sheet 7) is applied to the position loop amplifier circuit. Thus, the positioning of

Gate	Logical output	Function initiated	Display or end result observed
A33	1	Handwheel clutch solenoids are deenergized.	Handwheel positioning is disabled.
A18	1	MANUAL indicator is inhibited.	MANUAL indicator is extinguished.
A38A A38B	1	Followup resolver transfer relay K3 is deenergized.	Resolver output is applied to follow up loop.
A71	1	Azimuth followup brake L1 is deenergized.	Azimuth followup brakes are released, allowing followup to provide digital readout of antenna position.
A57	1	Elevation followup brake L1 is deenergized.	Elevation followup brakes are released, allowing followup to provide digital readout of antenna position.
A97	0	SIGNAL DETECT indicator is enabled.	SIGNAL DETECT indicator is illuminated.
A96B	1	One-half of dual low-level switch A103 (pins 7 and 10) is open.	Tach output is applied to position memory circuit.
A94A	0	One-half of dual low-level switch A103 (pins 3, 4, and 9) is closed.	Position memory caging is removed.
A111	0	PHASE LOCK indicator is enabled.	PHASE LOCK indicator is illuminated.
A110	0	AUTOTRACK indicator is enabled.	AUTOTRACK indicator is illuminated.
A112	1	ACQUISITION indicator is inhibited.	ACQUISITION indicator is extinguished.
A138	0	Track relay A13 is energized.	Tracking error signal is applied to position amplifier.

the antenna is limited to manual operation, while observing SIGNAL STRENGTH meter M1.

u. In the discussion of the followup disable mode (para 2-69), it was pointed out that the antenna control system returns to the manual mode of operation if phase lock is lost after depressing the FOLLOWUP DISABLE switch. This is a normal operation if a different satellite is to be acquired upon loss of a phase lock signal and if no attempt is to be made to reacquire the tracked satellite. However, phase lock can be lost due to signal conditions or other factors and reacquisition of the same satellite is desired. If the FOLLOWUP DISABLE switch has not been operated, the antenna control system reverts to the mode which existed prior to acquisition. The state of the control flip-flops is not dependent on phase lock logic; therefore, if phase lock is lost, the logic outputs revert to the state that existed prior to acquisition.

v. Azimuth and elevation brake relays K3 are deenergized and the brakes applied as discussed above. AZ BRAKE and EL BRAKE indicators DS1 and DS2 (sheet 6) on the power distribution panel are illuminated by the ground potential applied through the normally-closed contacts of the respective relay. When relay K4 is deenergized a ground is applied to illuminate OVERLOAD indicator DS3.

w. When relay K2 is deenergized a ground potential is applied to illuminate ANTENNA DRIVE indicator DS6. When the azimuth stow pin is inserted in the storage or operate hole, a ground is applied through AZ STOW LOCK switch S2 and terminal B of terminal board TB3 to illuminate STOW indicator DS5. When MOUNT SAFE switch S2 is actuated, the antenna control system is disabled and a ground is applied to illuminate MOUNT SAFE indicator DS4.

Section V. ANCILLARY EQUIPMENT

2-75. Analysis of Transmitter Cooling System
(fig. FO 2-10)

The transmitter cooling system is a liquid-to-air type heat transfer system utilizing on ethylene glycol and water coolant. The coolant mixture consists of 60 percent uninhibited ethylene glycol and 40 percent distilled water and is supplied at a minimum pump outlet pressure of 40 pounds-per-square-inch (psi). Coolant is pumped at a rate of 10 gallons per minute (gpm) and at a temperature of 63° C to 70° C (145° F to 158° F) while operating in ambient temperatures up to 49° C (120° F). The capacity of the system is approximately 3 gallons. Coolant carrying heat from the transmitter equipment is returned to the reservoir. The reservoir contains an air-space to allow for liquid expansion and a radiator-type pressure fill cap with a relief setting of 15 psi and the reservoir coolant level is monitored by two differential pressure switches.

a. Low liquid warning switch S1 is open and low liquid interlock switch S2 is closed when the coolant is at the proper level. Low liquid warning switch S1 closes when the coolant level drops to a 5-inch level and as a result, the LOW LIQUID WARNING indicator, on the transmitter control panel, illuminates. When the coolant level drops 3-1/2 inches, switch S2 opens and deenergizes a low liquid interlock relay which removes the transmitter and beam power.

b. The system centrifugal pump takes coolant by suction from the reservoir and discharges it, under pressure to one of three flow paths. One path is through the full flow three micron filter assembly through a particle filter coolant flow switch (S3) to the heat exchanger and temperature control value. Flow switch S3 is open until the coolant flow decreases to 7.5 gpm as a result of flow switch S3 closing, the LOW PARTICLE FIL. COOLANT FLOW indicator, on the transmitter control panel, illuminates to indicate that the filter is partially clogged. Another path is through the filter bypass valve to the heat exchanger and the temperature control valve. The last path is through the back flush valve to the temperature control valve and outlet of the heat exchanger. Thus, hot coolant is supplied direct from the pump to the temperature control valve and cold coolant is applied from the heat exchanger to the valve.

c. Cooling is achieved in the heat exchanger by the fan drawing ambient air through the heat exchanger and exhausting it out through the fan orifice. The temperature control valve senses the output coolant temperature and automatically mixes hot and cold coolant to provide a constant flow of fluid between 63° C and 70° C (145° F and 158° F) to the transmitter equipment. The coolant temperature and pressure are sensed at the outlet of the temperature control valve, and the values are displayed on gauges located on the heat transfer system panel.

d. A portion of coolant (12 GPH) from the pump is directed through a conductivity cell and a flow meter to

the deionizer. The deionizer removes ions, minerals, and oxygen from the coolant. The treated coolant is returned to the reservoir through a .35 micron filter, a second conductivity cell and a flow control orifice.

e. The coolant from the temperature control valve is applied to a manifold for distribution to the transmitter equipment. The coolant temperature is monitored by thermostatic switches S1 and S2. Provided the coolant temperature is below 68° ± 3° C (154° ± 5° F), high coolant temperature switch S1 is closed. In this condition system coolant high temperature relay K21 (fig. FO 2-4, sheet 3) is energized. When the coolant reaches a temperature of 73° ± C (163.5 ± 3.5° F), switch S1 opens and relay K21 is deenergized. As a result, the transmitter control panel HIGH COOL TEMP indicator illuminates.

f. Provided the coolant temperature is above 1° ± 2° C (34 ± 4° F), low coolant temperature switch S2 is open. If the coolant temperature drops below -4.5° ± 2° C (24 ± 4° F), switch S2 closes and initiates two actions. First, the LOW COOL TEMP indicators, on the transmitter control panel and frequency multiplier 1A3A6, illuminate. Second, liquid heater relay K1 is energized, which applies power to heater HR1 and the coolant from the manifold is heated to compensate for extreme cold ambient temperatures. A pressure relief valve on the heater is set to operate at 200 psi.

g. Coolant flow through the transmitter equipment is monitored by flow switches S3, S4, S5, and S6 (fig. FO 2-4, sheet 3). Fluid must flow through waveguide and dummy load switch S4 and body at a rate in excess of one gallon per minute and magnet switches S3 and S6 at a rate in excess of .5 gallons per minute. Flow through collector switch S5 must exceed 5 gpm. When the coolant flow through switch S3 or S6 drops below .5 gpm, the switch opens as shown in figure FO 2-4, sheet 3 and body and magnet flow relay K18 is deenergized and, the transmitter control panel BODY AND MAG FLOW indicator lamp illuminates. When coolant flow drops below the prescribed valve through switches S4 and S5, corresponding indicators on the transmitter control panel illuminate. Provided the flow through the two switches is adequate, flow switch relay K19 is energized with the results discussed in paragraph 2-24.

2-76. Analysis of Waveguide Pressurization System
(fig. FO 2-11)

Dry, clean, low pressure air is supplied to the microwave components of the AN/TSC-54 by a compressor-dehydrator. The purpose of the dry air is to prevent moisture from collecting in the waveguides.

a. The dry and filtered air is routed through a manually operated flow valve when the valve is in the DEHYDRATOR position. The air is then applied to four indicator-flow valves. When the manually-operated flow valve is in the NITROGEN position; dry nitrogen, applied to the AUXILIARY DRY NITROGEN INPUT, can replace the compressor-dehydrator.

b. The four indicator-flow valve inputs are connected in paralled to the manually operated flow valve. These valves regulate and indicate the amount of air supplied to three areas of the microwave system. The fourth valve supplies an air sample to a HUMIDITY indicator located on the indicator-air monitor panel.

c. Each of the indicator-flow valves has a movable red pointer which is set to indicate the proper rate of air flow through the systems. The rate of air flow in each valve is adjusted by turning the associated knob, located at the bottom, until the ball in the tube rises to the proper level.

d. The air for the receive elliptical waveguide is routed through the RCVR flow valve. An adjustable bleed valve is located at the shelter ends of the waveguide. This bleed valve is adjusted in conjunction with the flow-valve knob (*c* above) to regulate air flow through the waveguide.

e. The air flow for the transmit elliptical waveguide is routed through the DRIVER flow valve. The transmit waveguide has a bleed valve at the shelter end and is used in the same manner as the receive side (*d* above).

f. The air for the antenna and pedestal microwave components is routed through the HPA flow valve. The output of this valve is routed to a filtering in the waveguide adapter connected to the reverse power part of directional coupler DC3.

2-77. Analysis of Intercommunication System
(fig. FO 2-12)

The AN/TSC-54 intercommunication system is a 4-wire, two-way voice communication system which provides intercommunication between the inside of the electronic equipment shelter and selected areas of the antenna pedestal.

a. Telephone jack J1 in the electronic equipment shelter is connected through jack J7 of primary power distribution panel 2A3A14 and filters FL5A4, FL5B2, FL6B4 and FL6C1 to the following selected areas of the

antenna pedestal to jack J101 of antenna pedestal 2A3, to jack J1 of rf box 2A9A1 (through filters FL3C3, FL3C4, FL4A2 and FL4A3 of elevation cable wrap assembly 2A5), and to jacks J1 through J4 on intercom/air monitor panel 2A3A24. By patching into the telephone jacks, two or all jacks can be combined into a single loop for conversations between several parties.

b. Intercom control unit 2A3A24A1 (C-611D/A1C) contains a single receive and a single transmit amplifier which provides a suitable single level for use. For detailed description of the intercom unit reference TM 11-5831-35.

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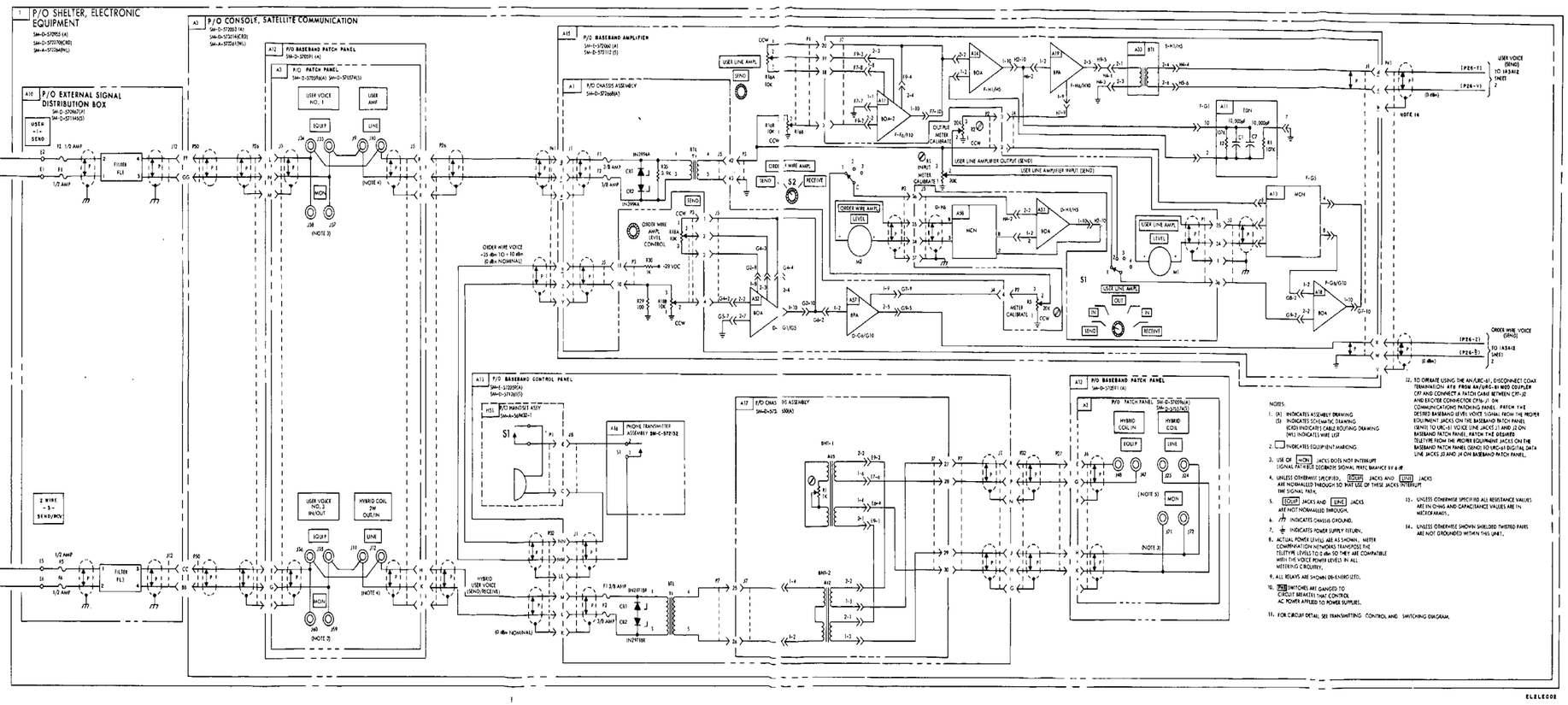

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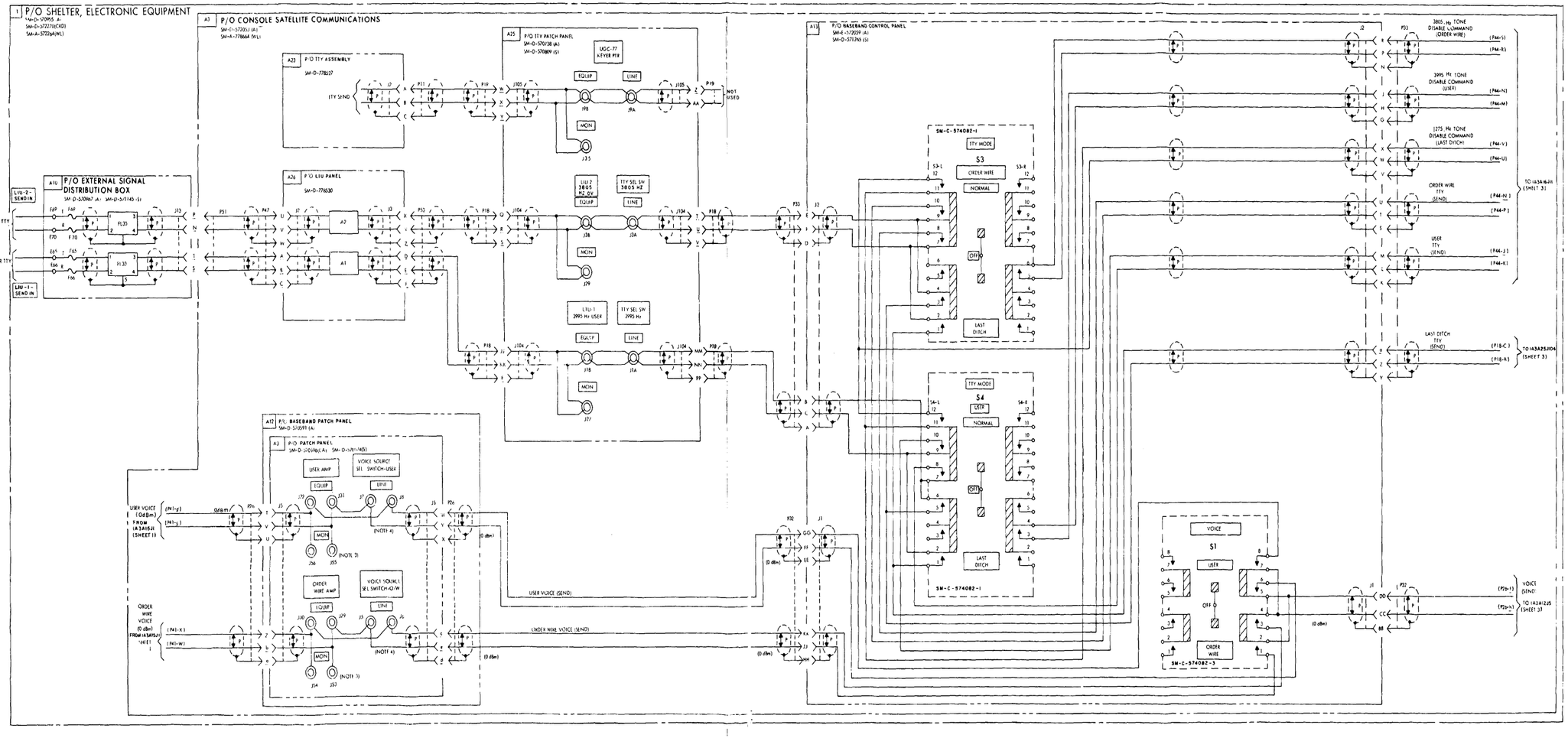

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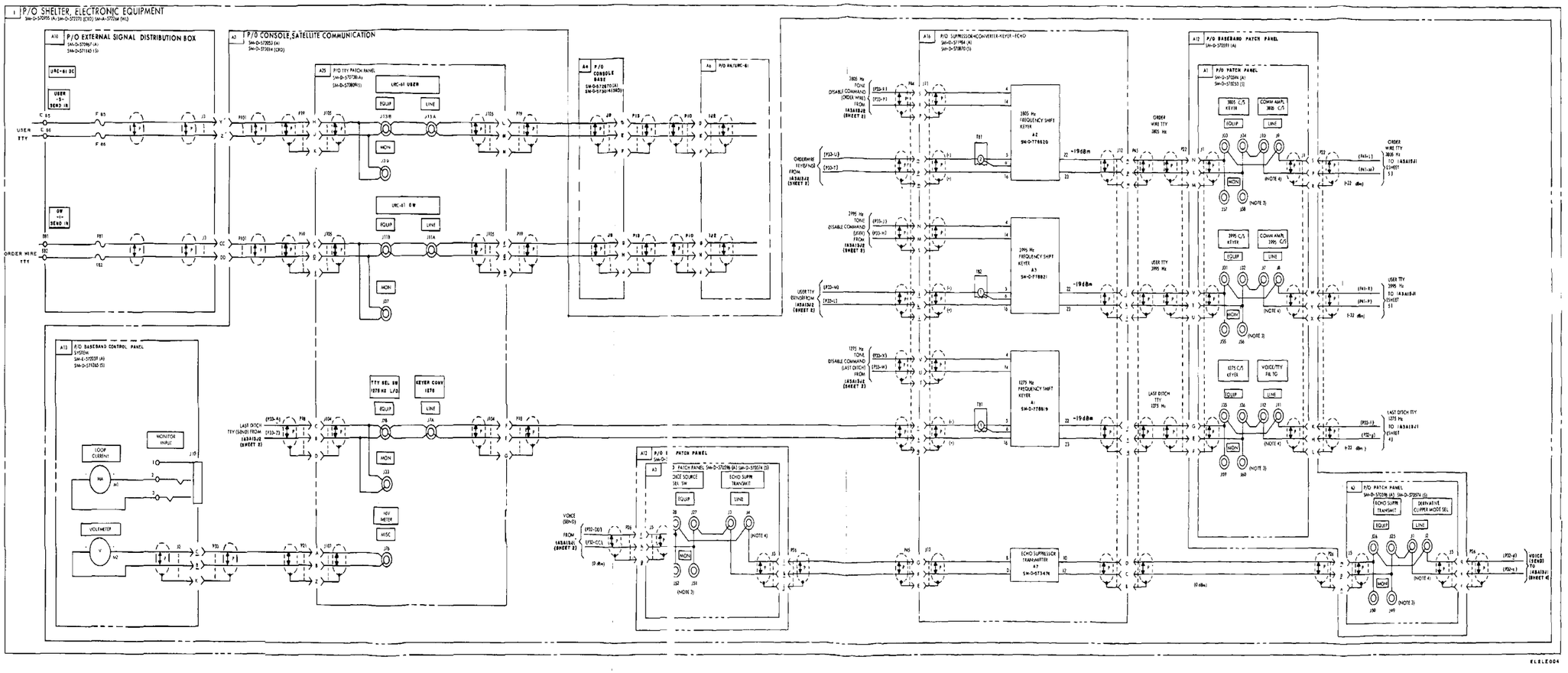

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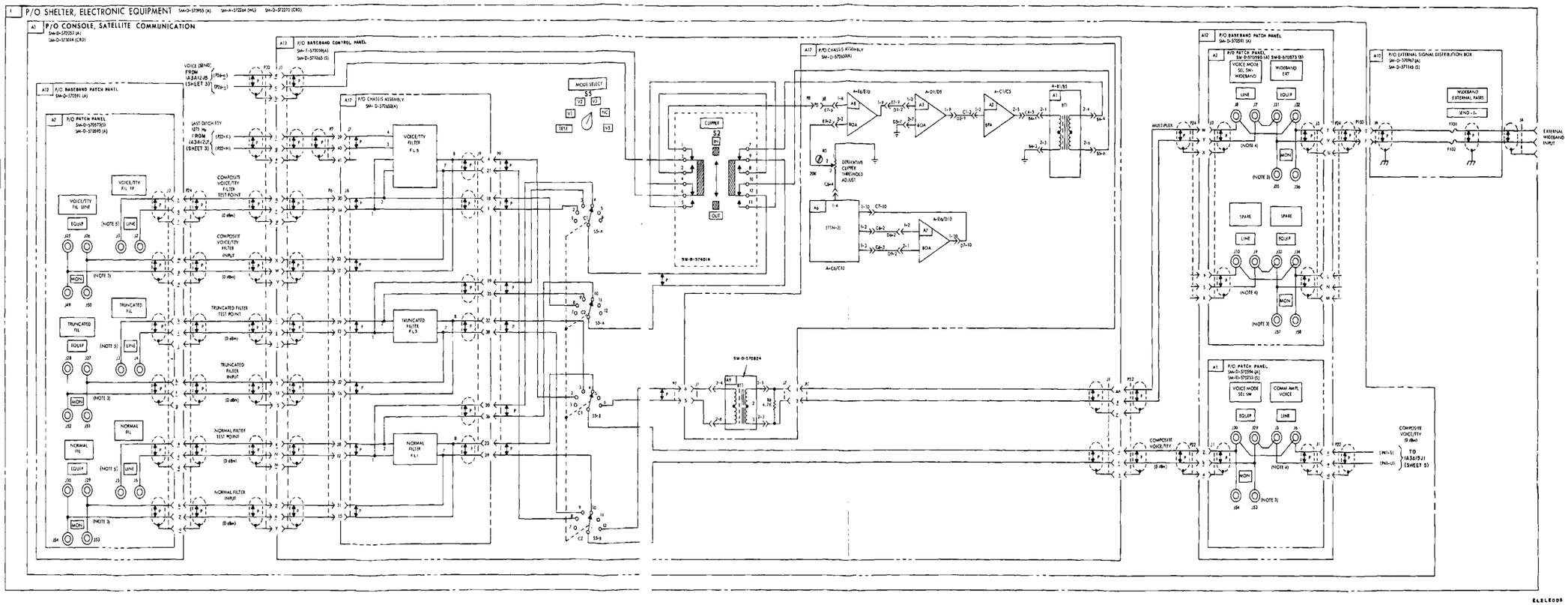

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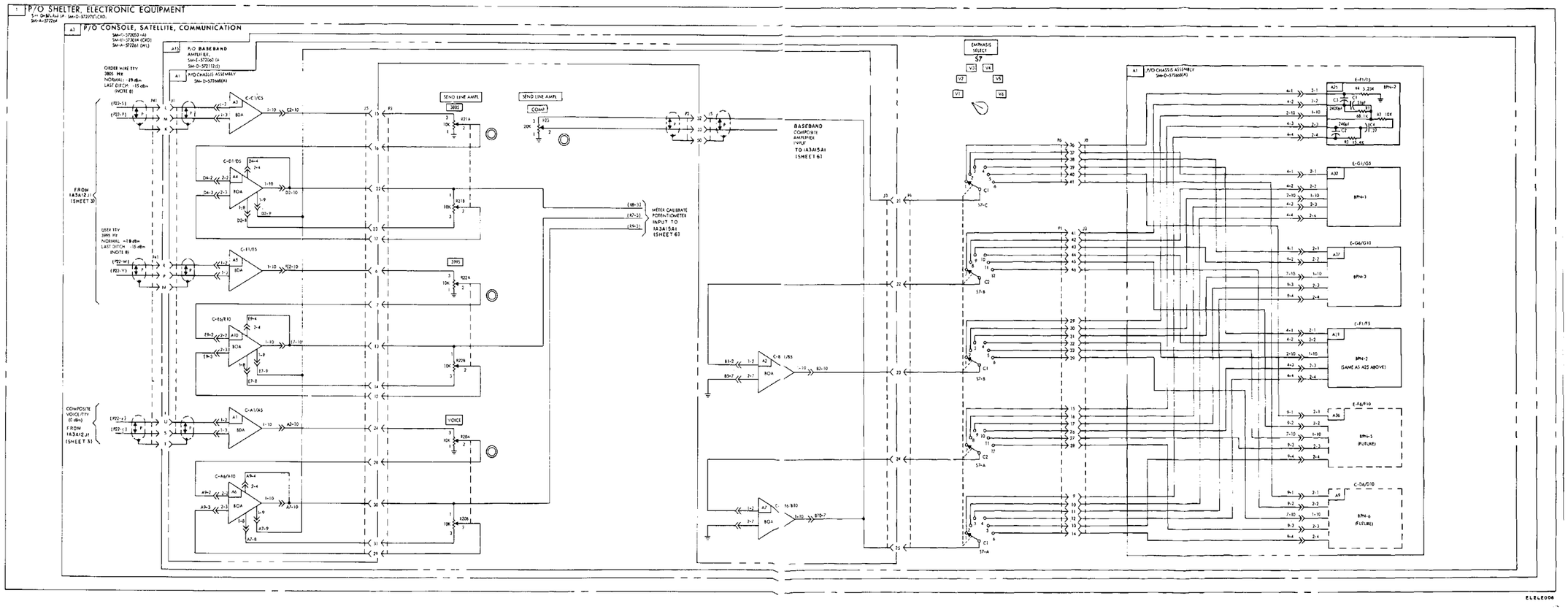

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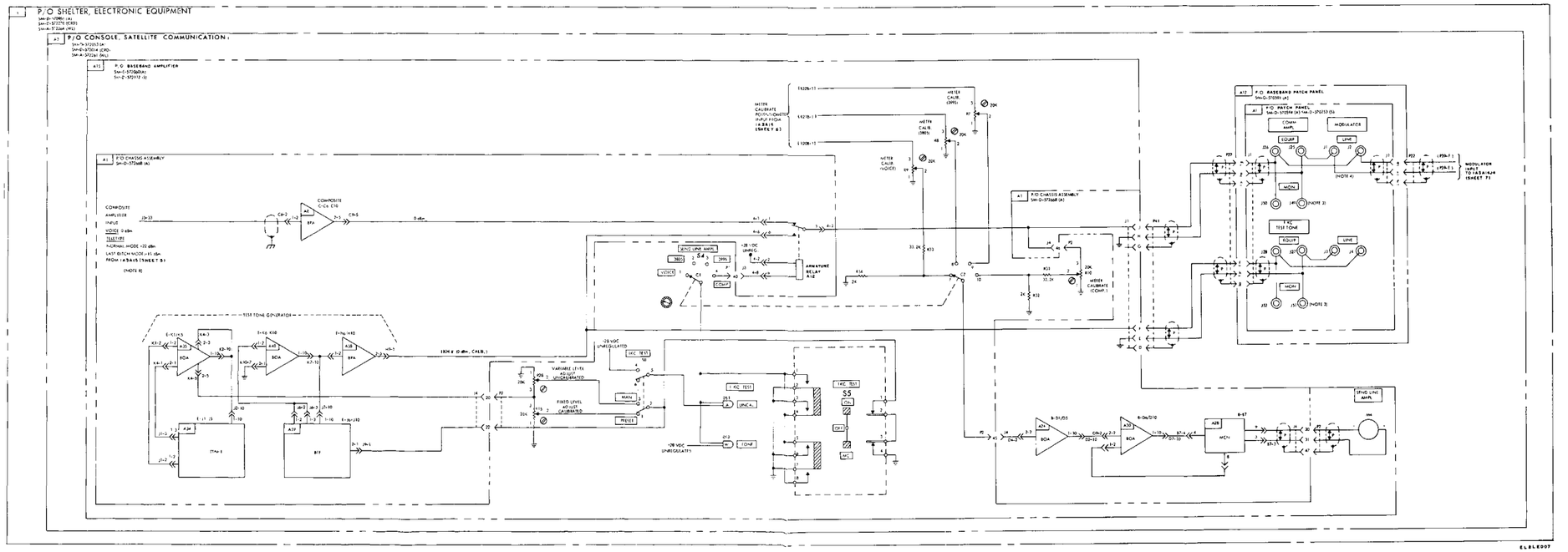

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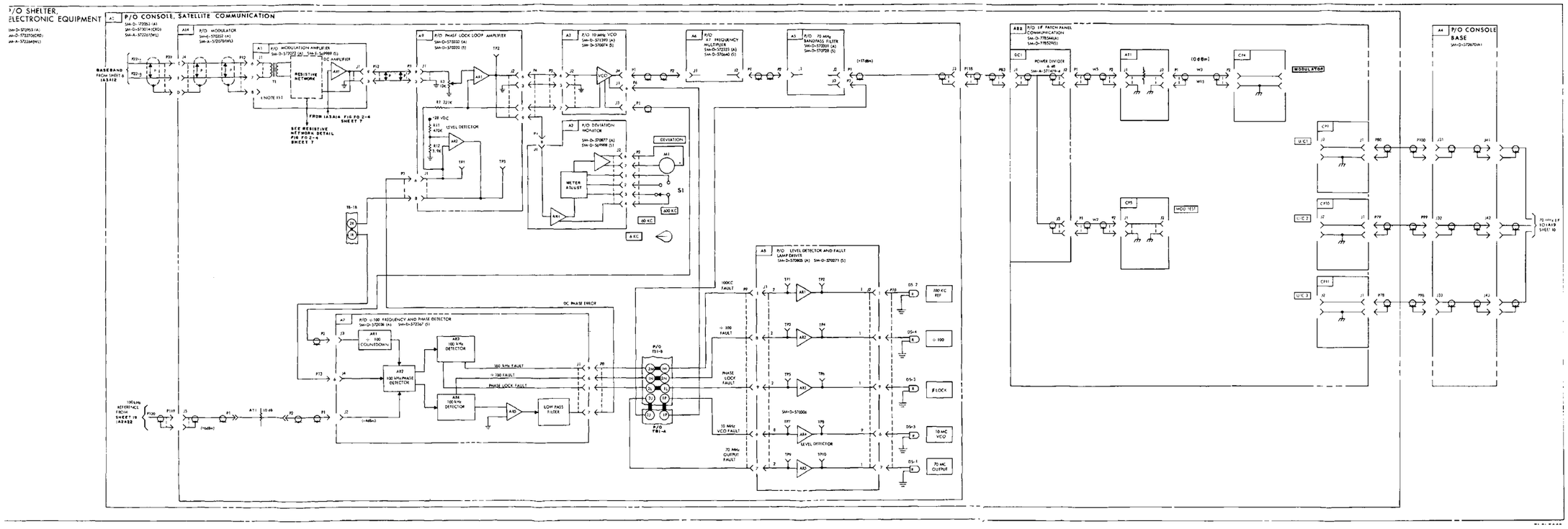

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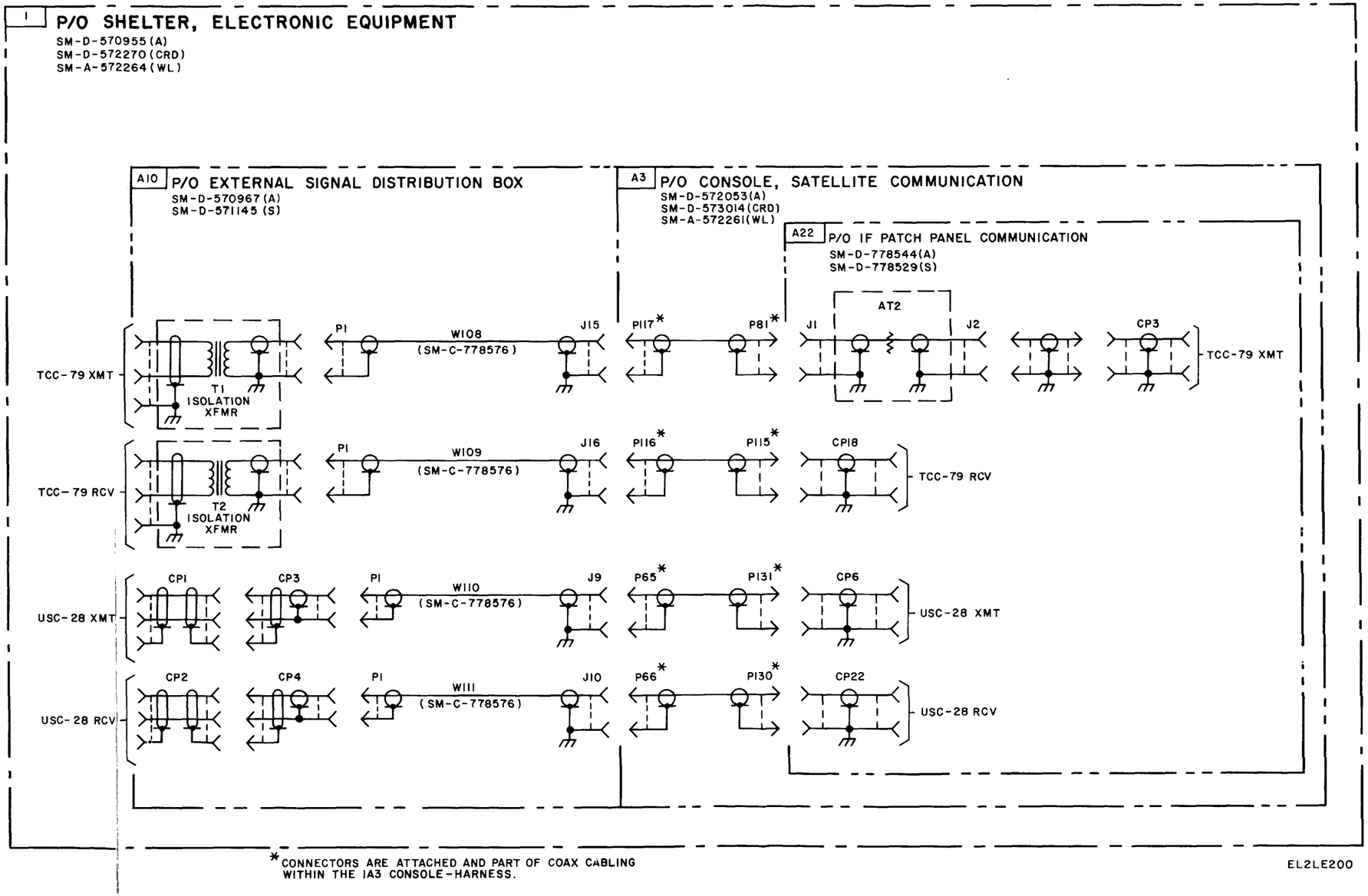

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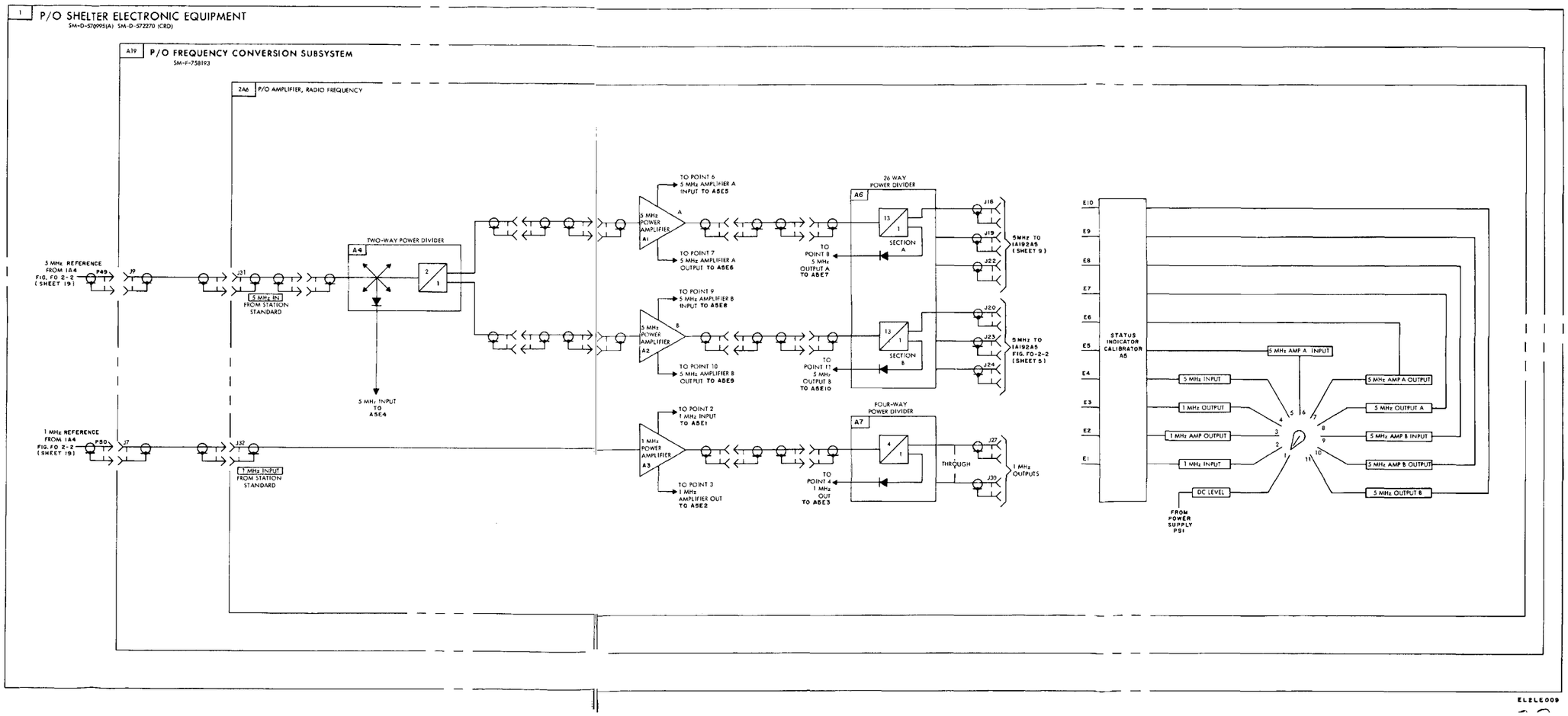

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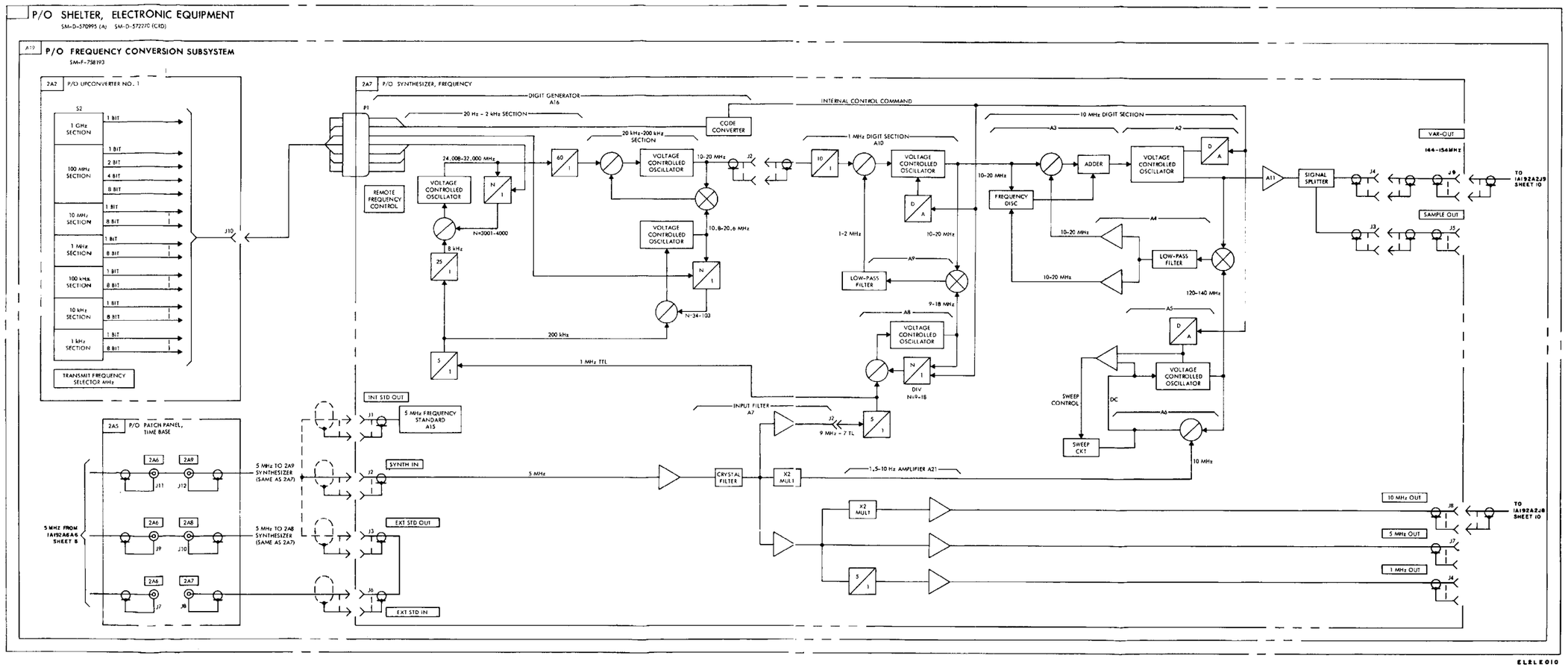

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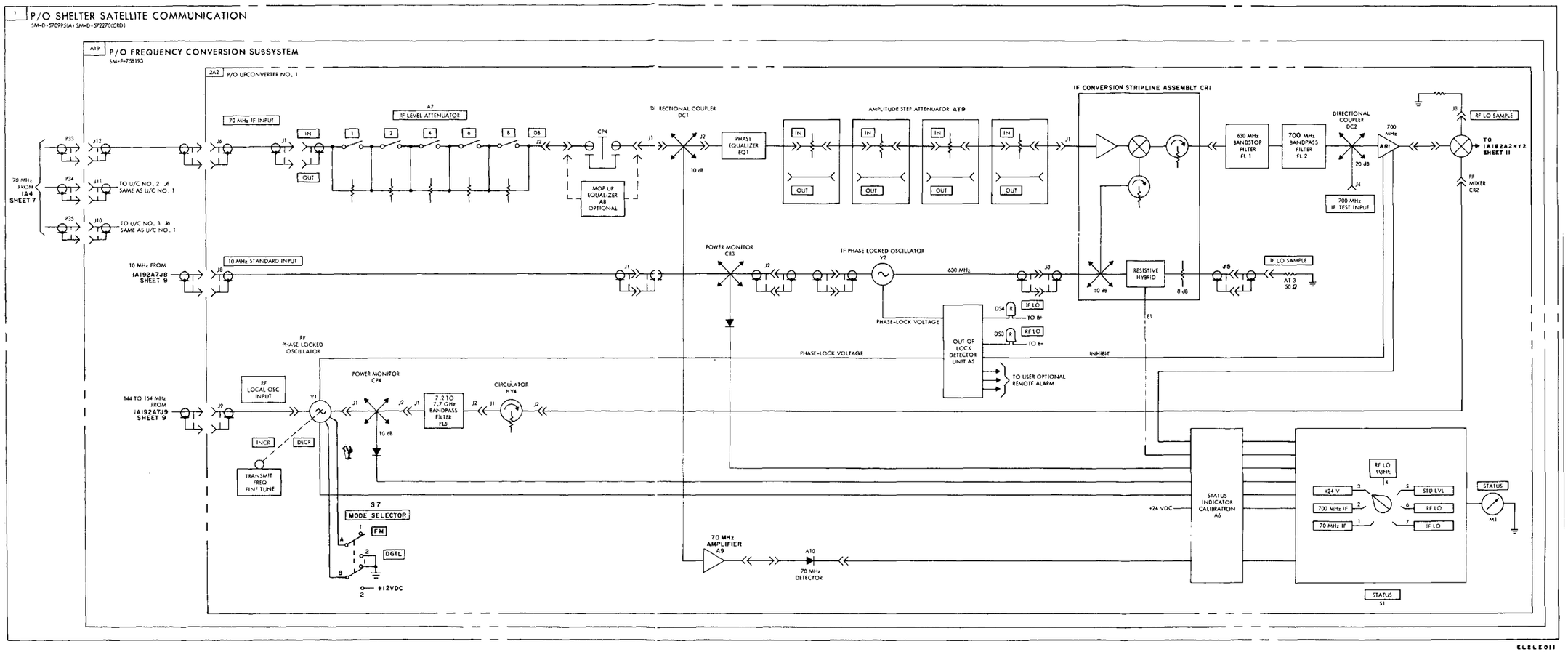

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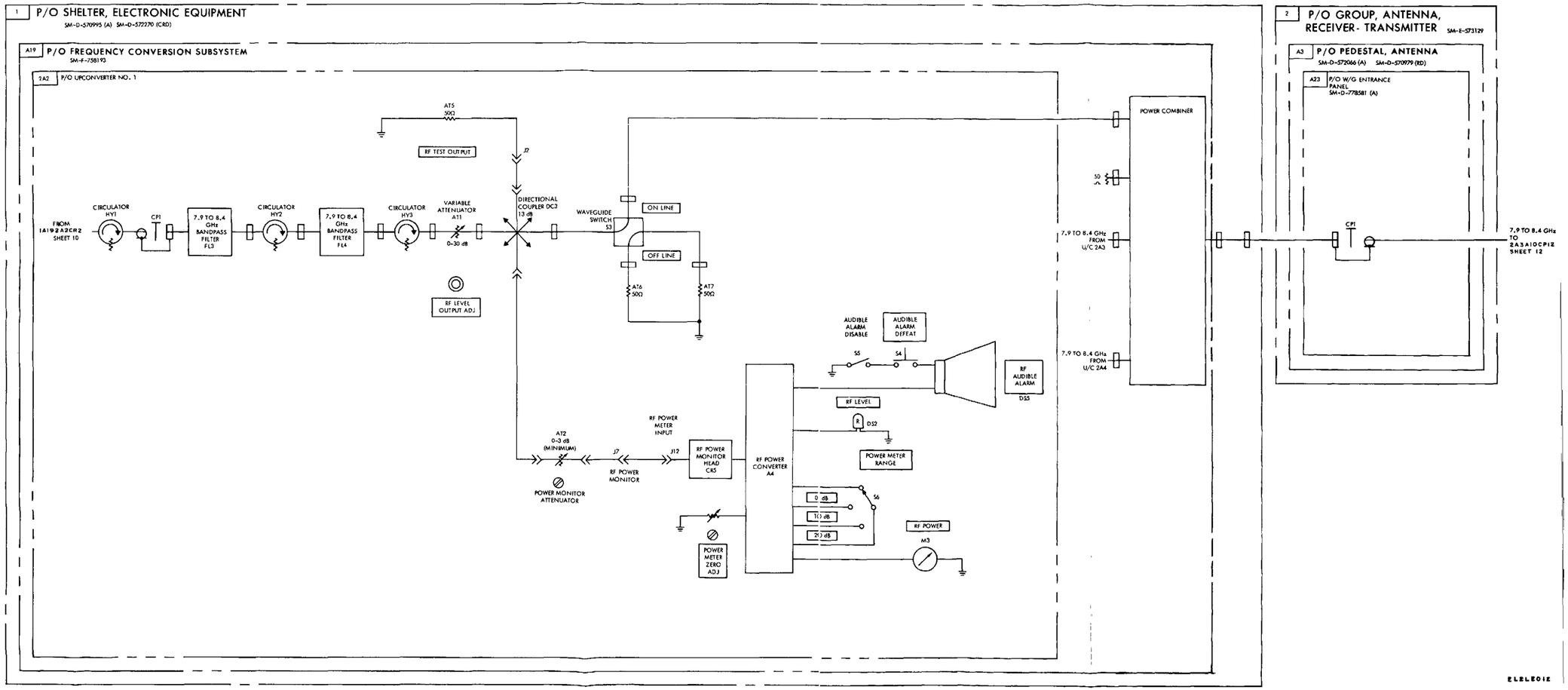

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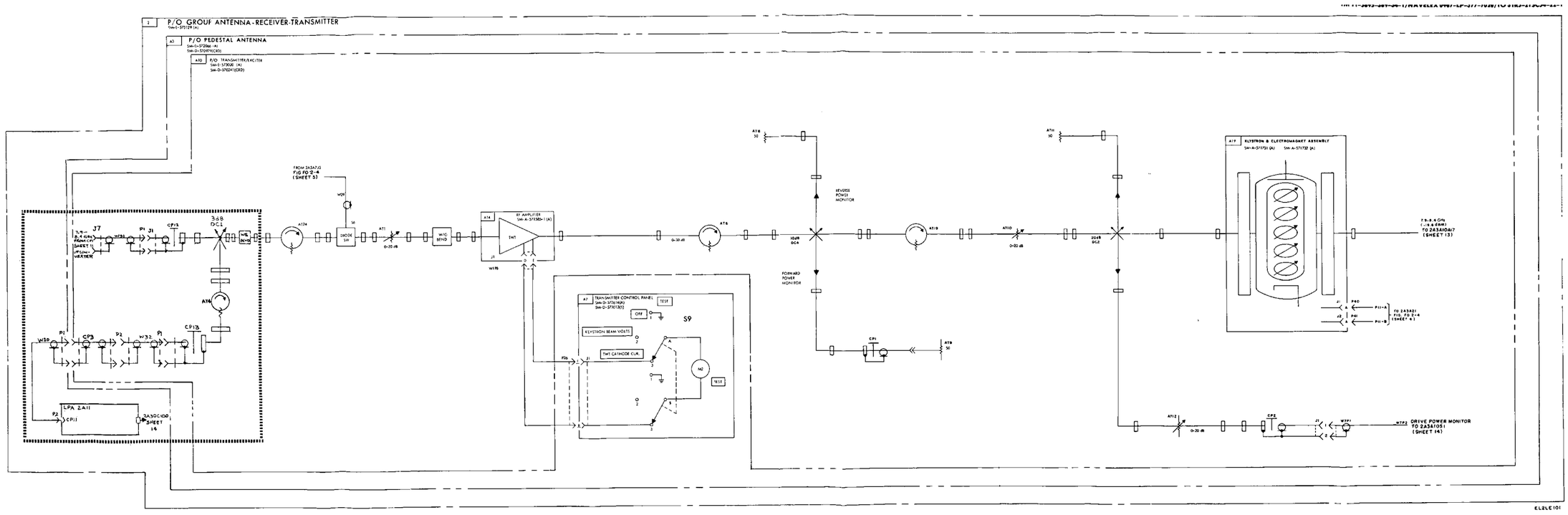

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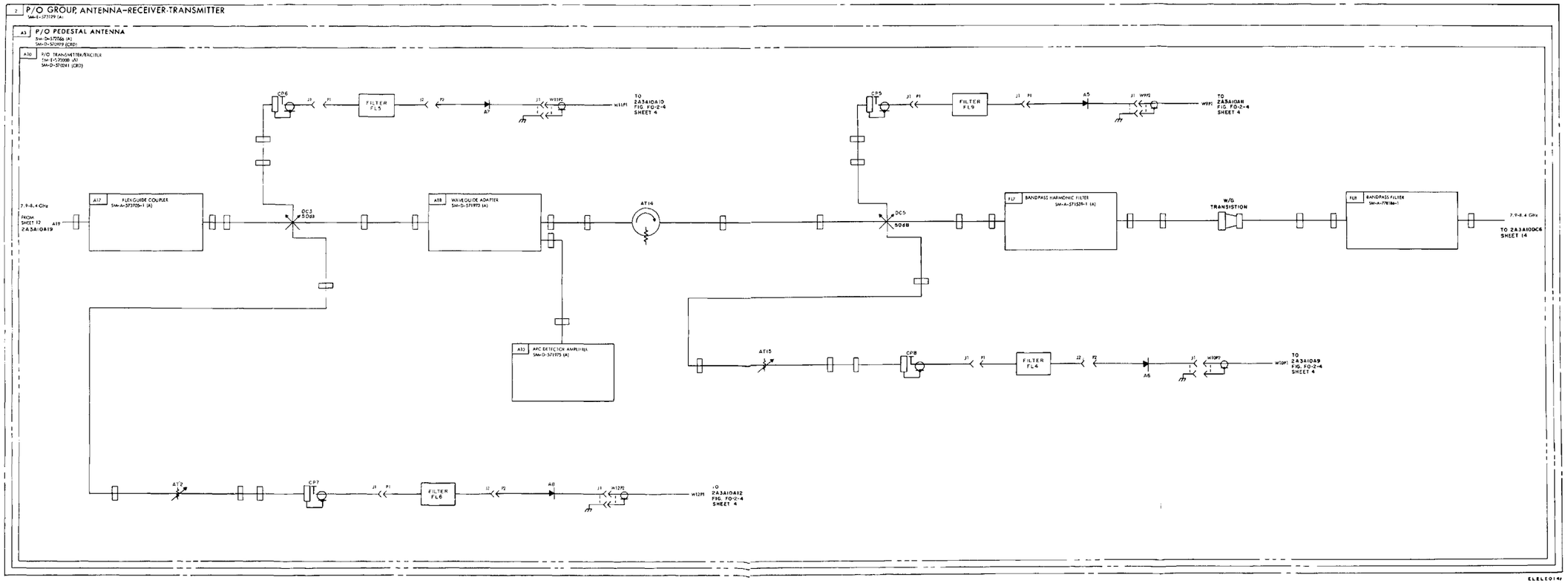

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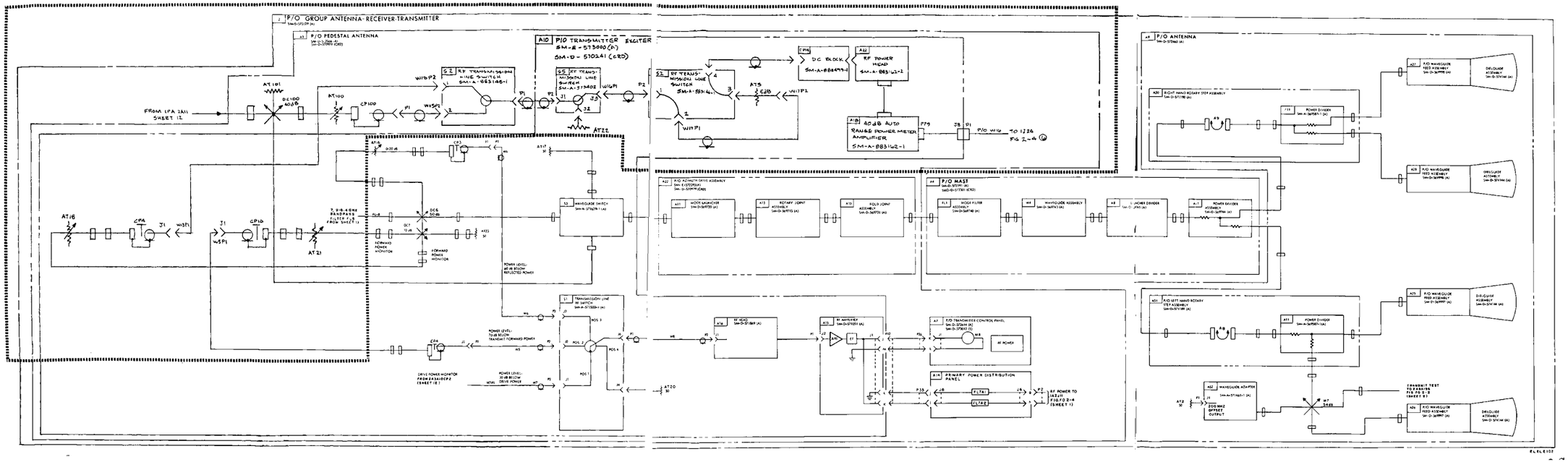

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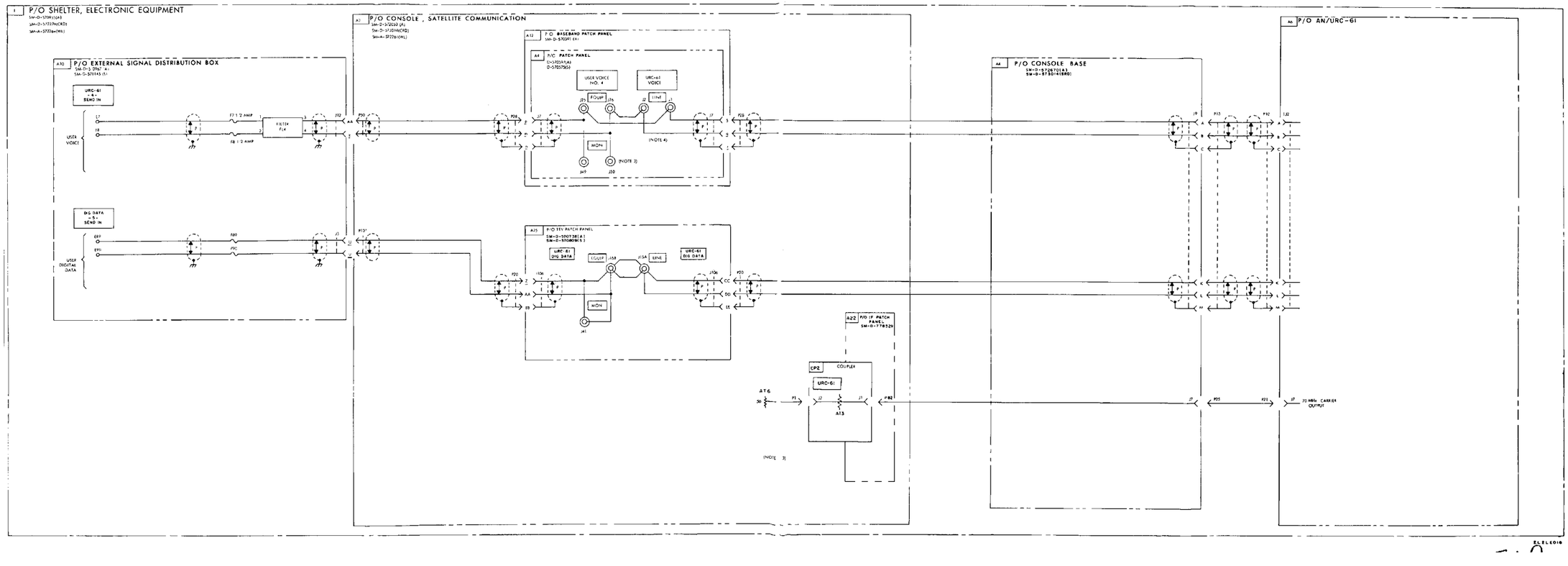

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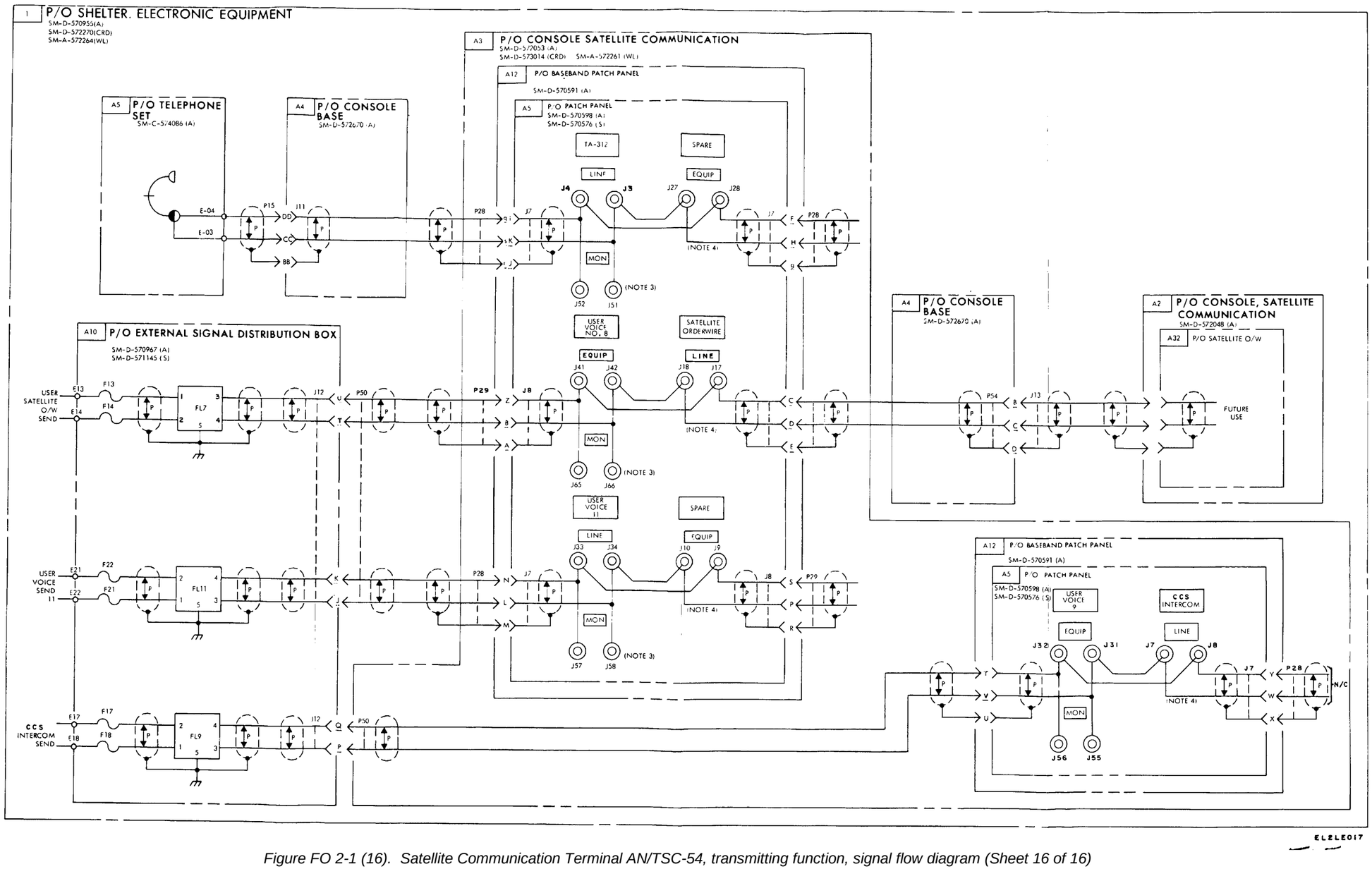

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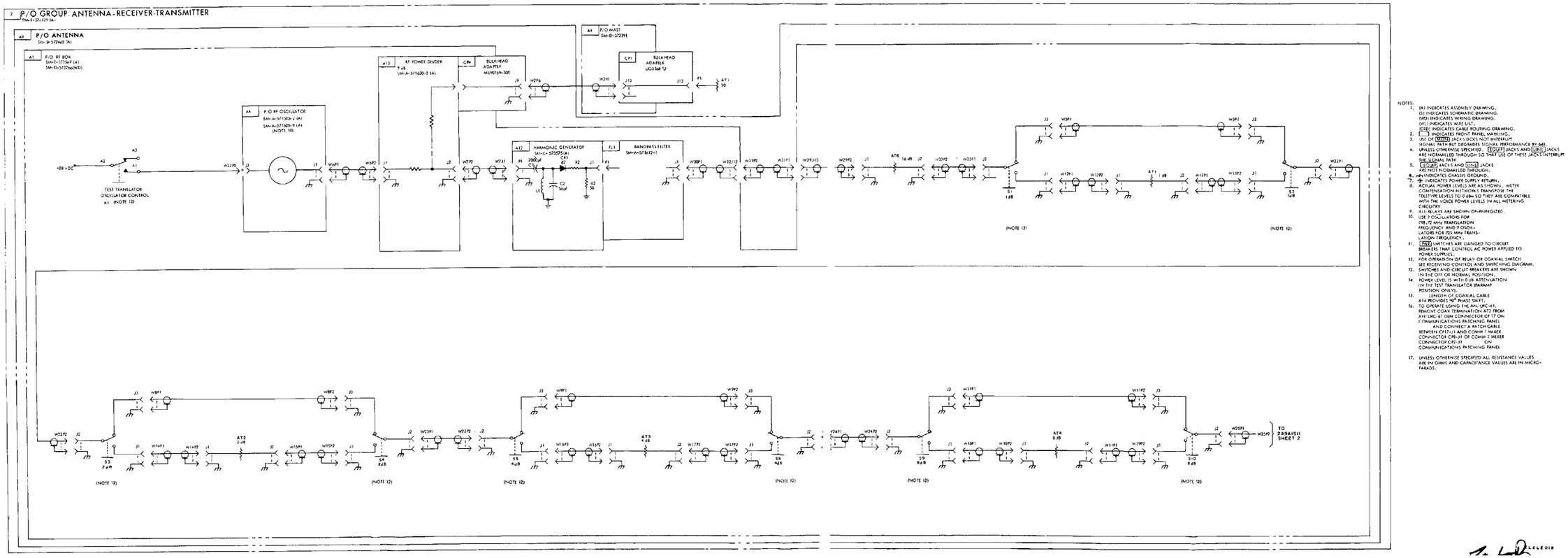
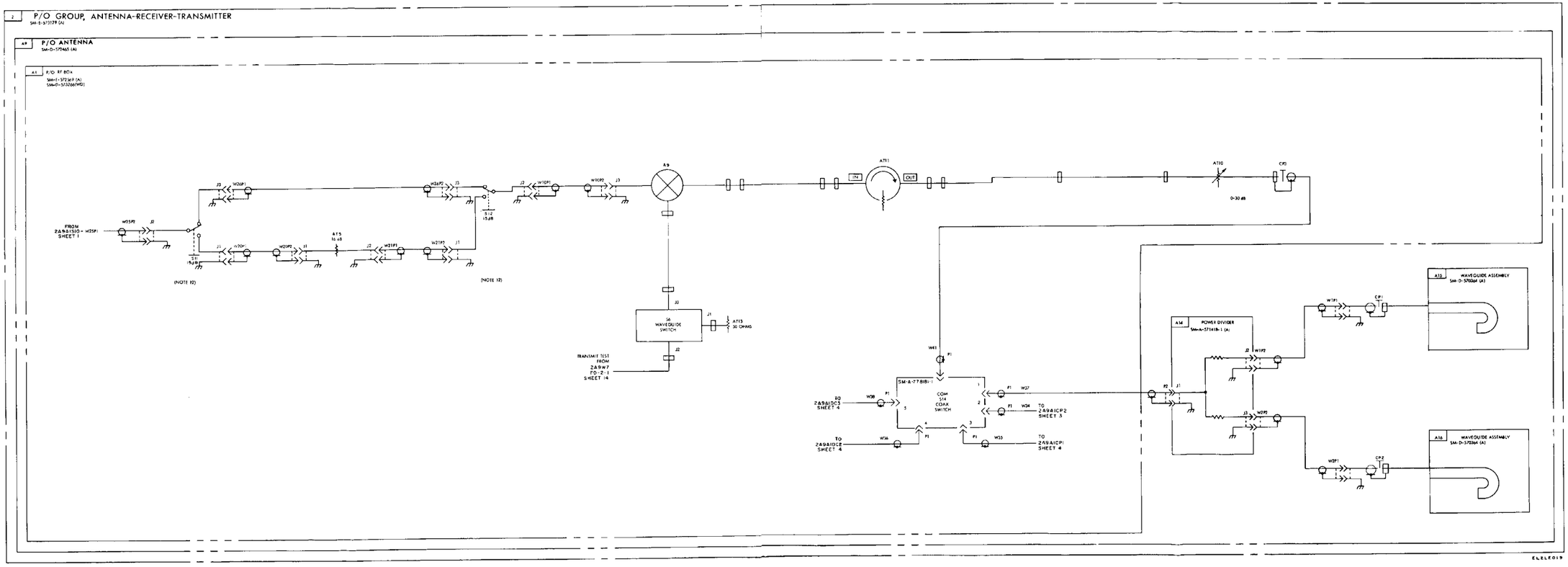


NOTES:

1. (A) INDICATES ASSEMBLY DRAWING.
   (S) INDICATES SCHEMATIC DRAWING.
   (WD) INDICATES WIRING DRAWING.
   (WL) INDICATES WIRE LIST.
   (CRD) INDICATES CABLE ROUTING DRAWING.
2. [ ] INDICATES FRONT PANEL MARKING.
3. USE OF [MONO] JACKS DOES NOT INTERRUPT SIGNAL PATH BUT DEGRADES SIGNAL PERFORMANCE BY 6dB.
4. UNLESS OTHERWISE SPECIFIED, [EQUIP] JACKS AND [LINE] JACKS ARE NORMALLED THROUGH SO THAT USE OF THESE JACKS INTERRUPT THE SIGNAL PATH.
5. [EQUIP] JACK 5 AND [LINE] JACKS ARE NOT NORMALLED THROUGH.
6. ⏚ INDICATES CHASSIS GROUND.
7. ⏚ INDICATES POWER SUPPLY RETURN.
8. ACTUAL POWER LEVELS ARE AS SHOWN. METER COMPENSATION NETWORKS TRANSPOSE THE TELETYPE LEVELS TO 0 dBm SO THEY ARE COMPATIBLE WITH THE VOICE POWER LEVELS IN ALL METERING CIRCUITRY.
9. ALL RELAYS ARE SHOWN DE-ENERGIZED.
10. USE 2 OSCILLATORS FOR 718.72 MHz TRANSLATION FREQUENCY AND 2 OSCILLATORS FOR 723 MHz TRANSLATION FREQUENCY.
11. [PWR] SWITCHES ARE GANGED TO CIRCUIT BREAKERS THAT CONTROL AC POWER APPLIED TO POWER SUPPLIES.
12. FOR OPERATION OF RELAY OR COAXIAL SWITCH SEE RECEIVING CONTROL AND SWITCHING DIAGRAM.
13. SWITCHES AND CIRCUIT BREAKERS ARE SHOWN IN THE OFF OR NORMAL POSITION.
14. POWER LEVEL IS WITH 0 dB ATTENUATION IN THE TEST TRANSLATOR (RAMP POSITION ONLY).
15. LENGTH OF COAXIAL CABLE A14 PROVIDES 90° PHASE SHIFT.
16. TO OPERATE USING THE AN/URC-61, REMOVE COAX TERMINATION AT3 FROM AN/URC-61 ITEM CONNECTOR OF 17 ON COMMUNICATIONS PATCHING PANEL AND CONNECT A PATCH CABLE BETWEEN CP17-J3 AND COMM 1 MIXER CONNECTOR CP6-J1 OR COMM 2 MIXER CONNECTOR CP6-J1 ON COMMUNICATIONS PATCHING PANEL
17. UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.

Figure FO 2-2. (1). Satellite Communication Terminal AN/TSC-54, receiving function, signal flow diagram (Sheet 1 of 19)



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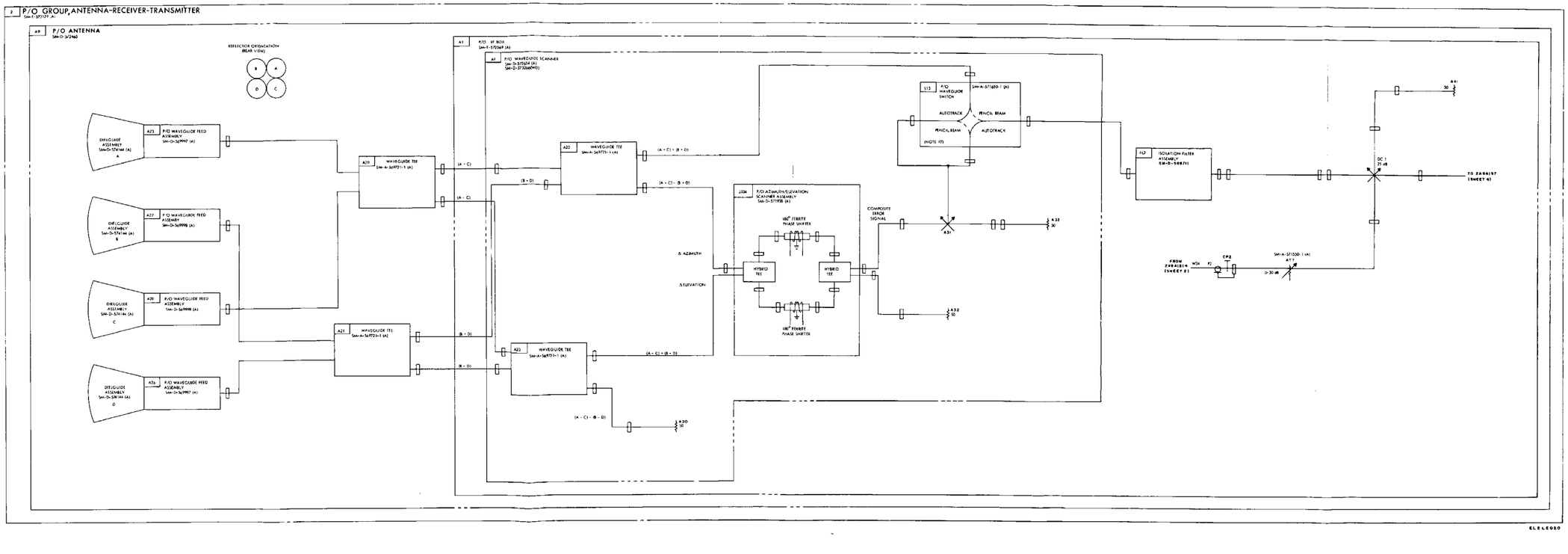

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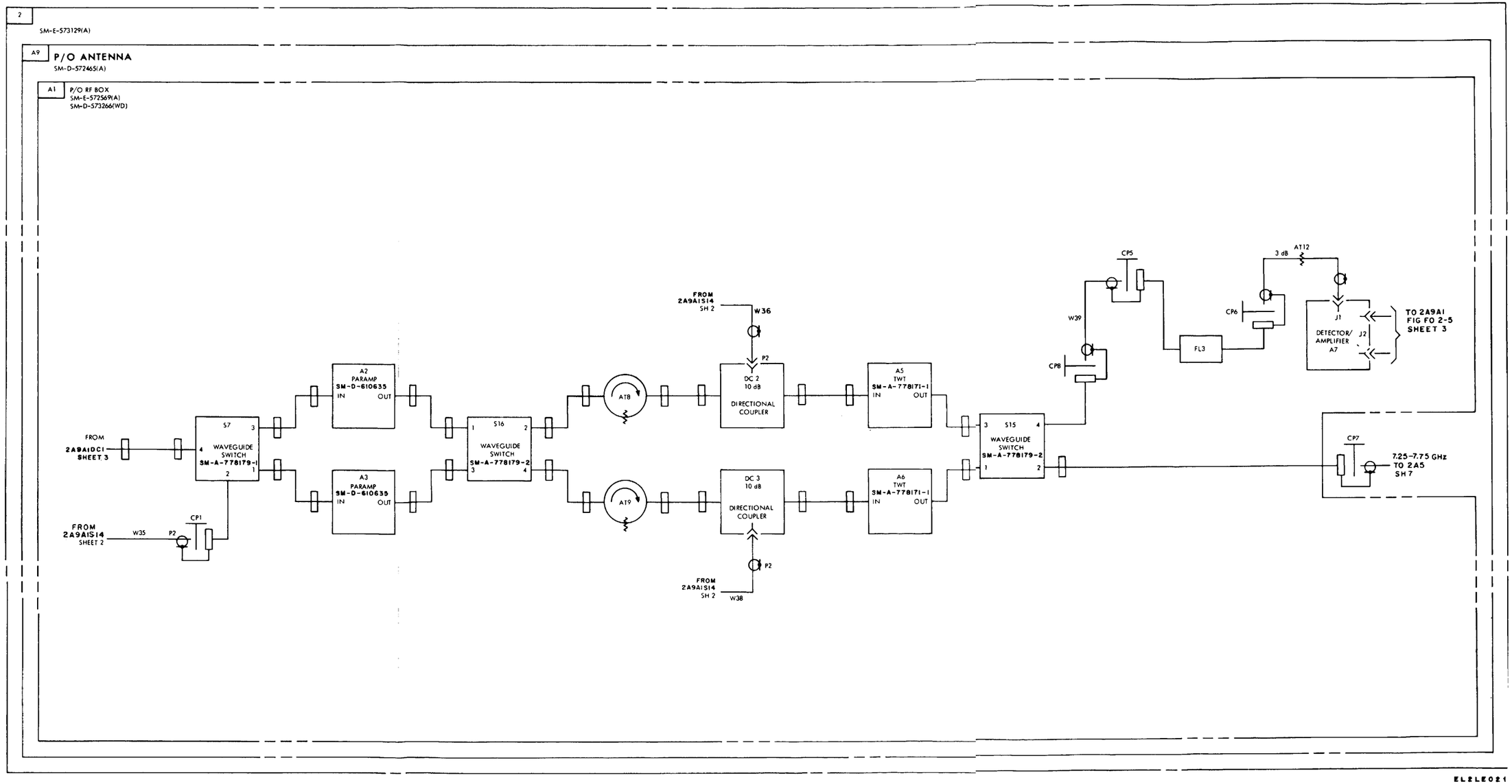

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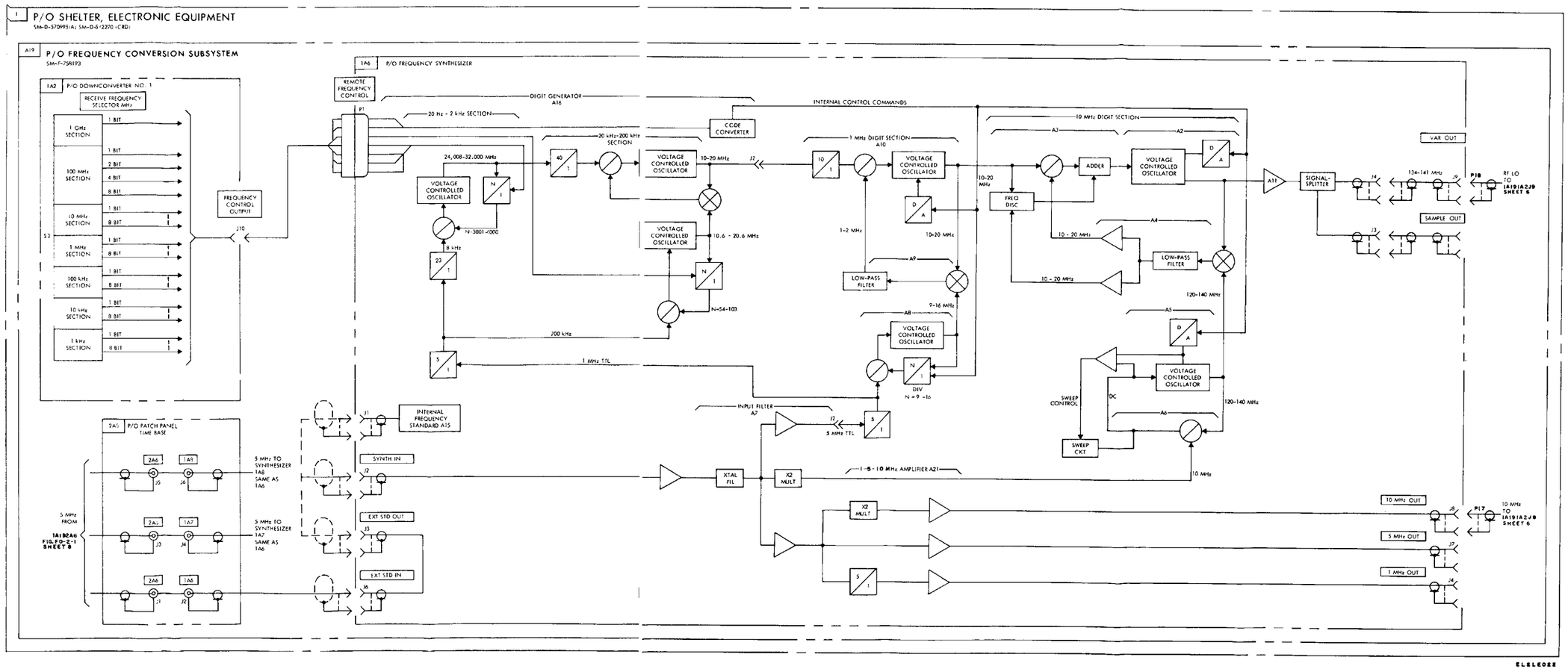

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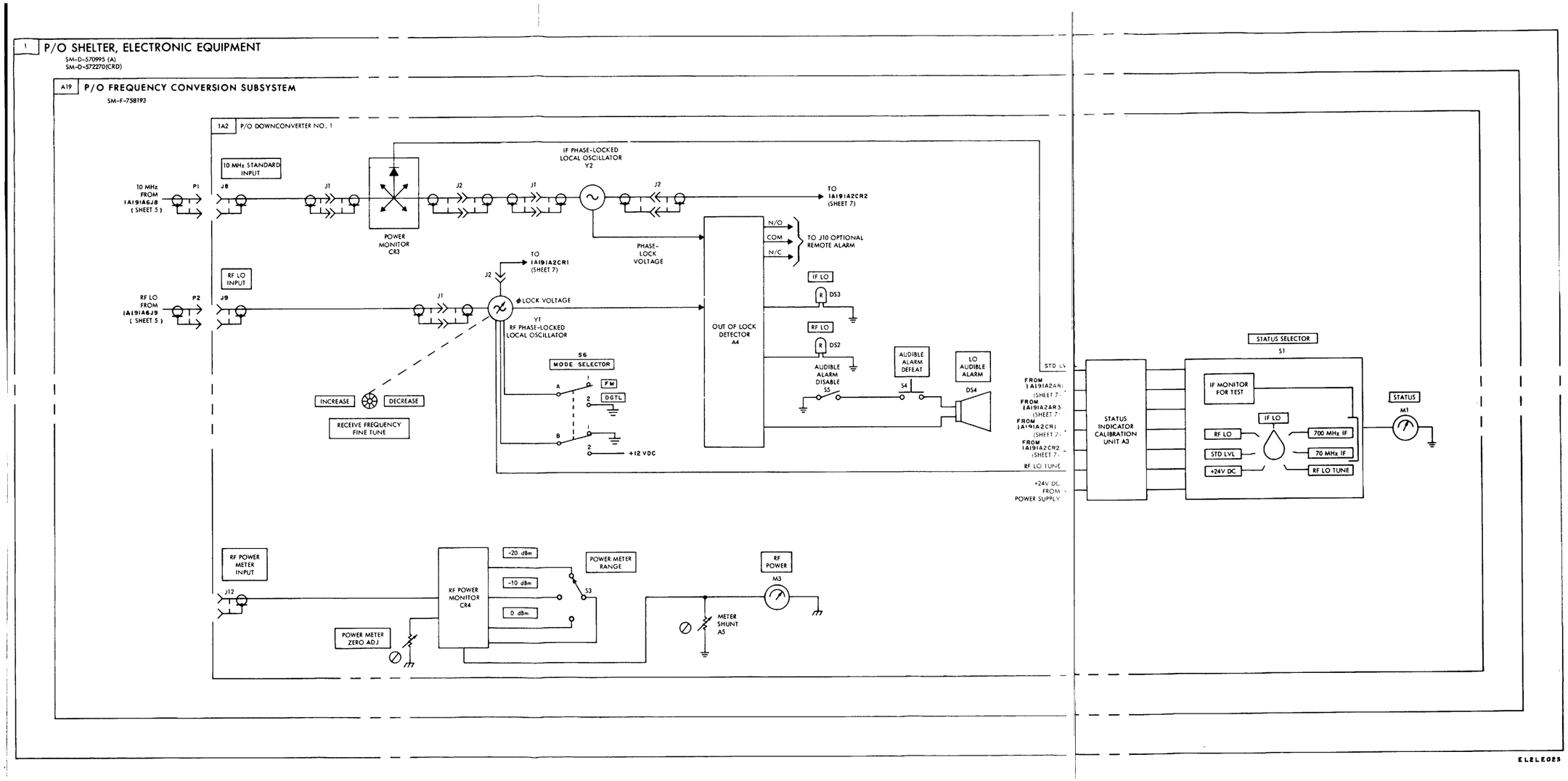

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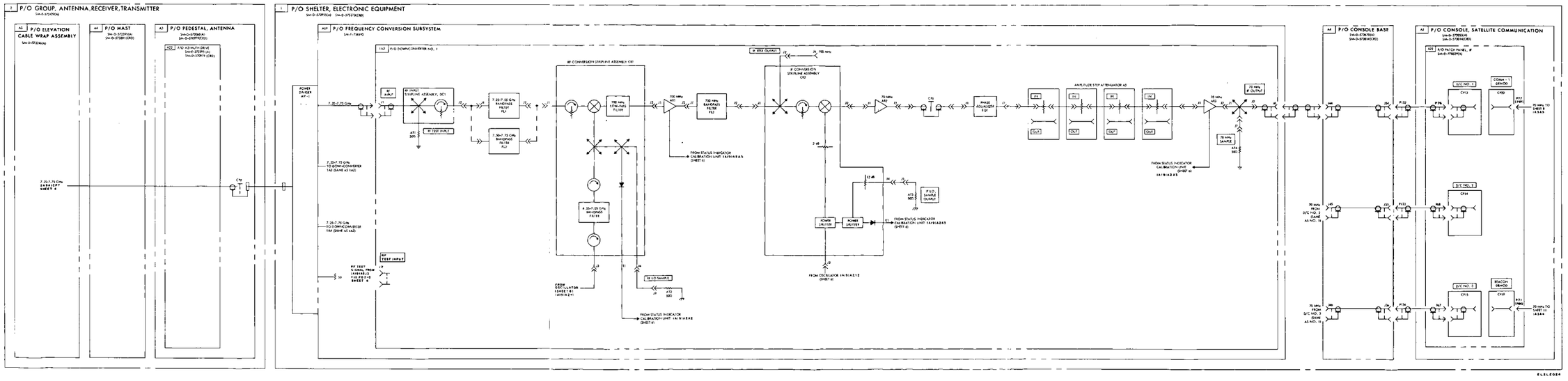

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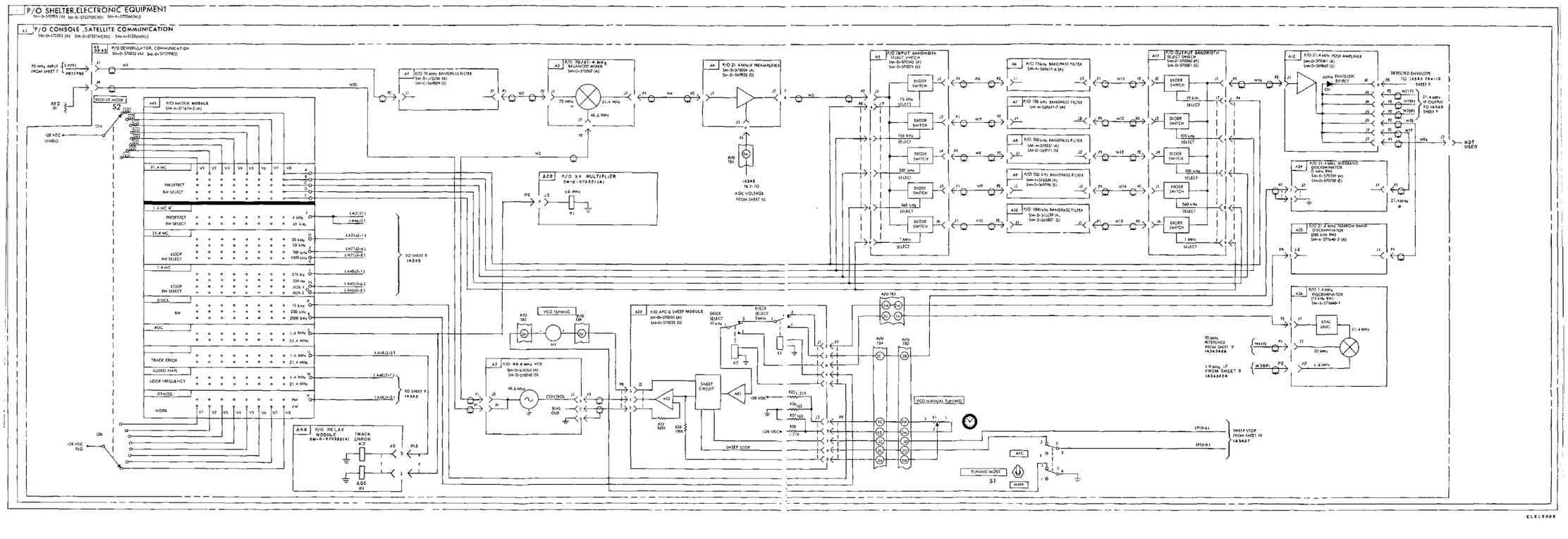

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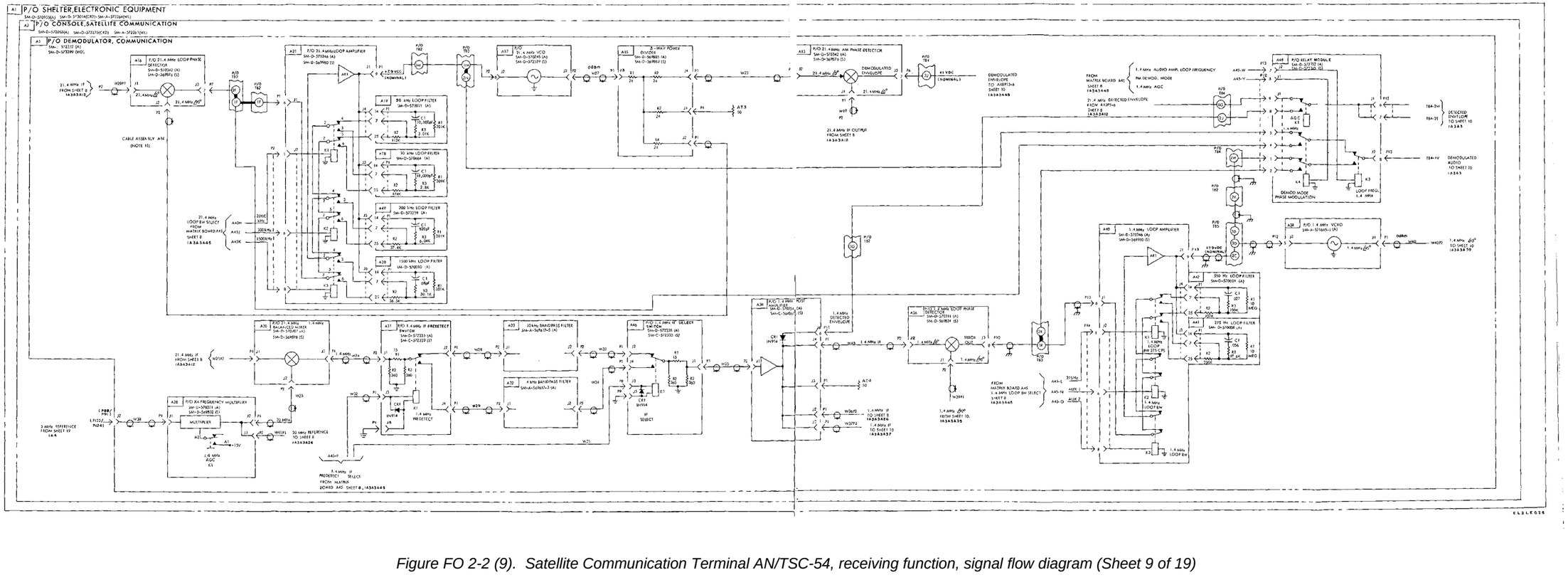

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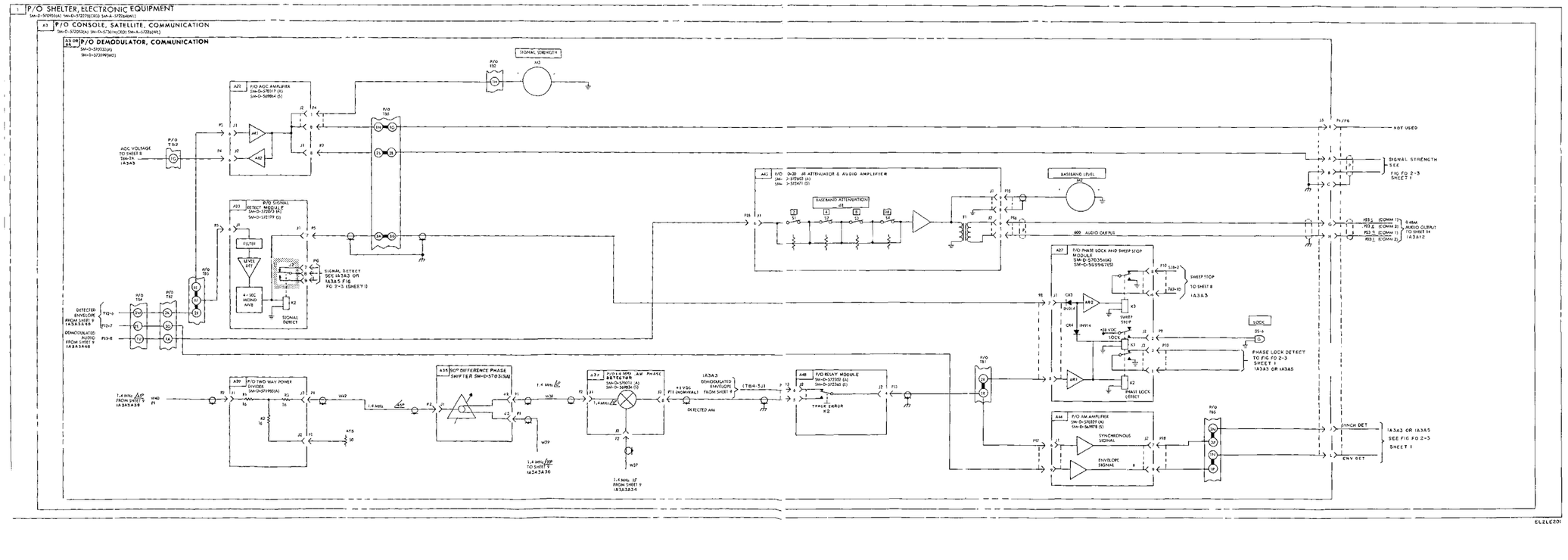

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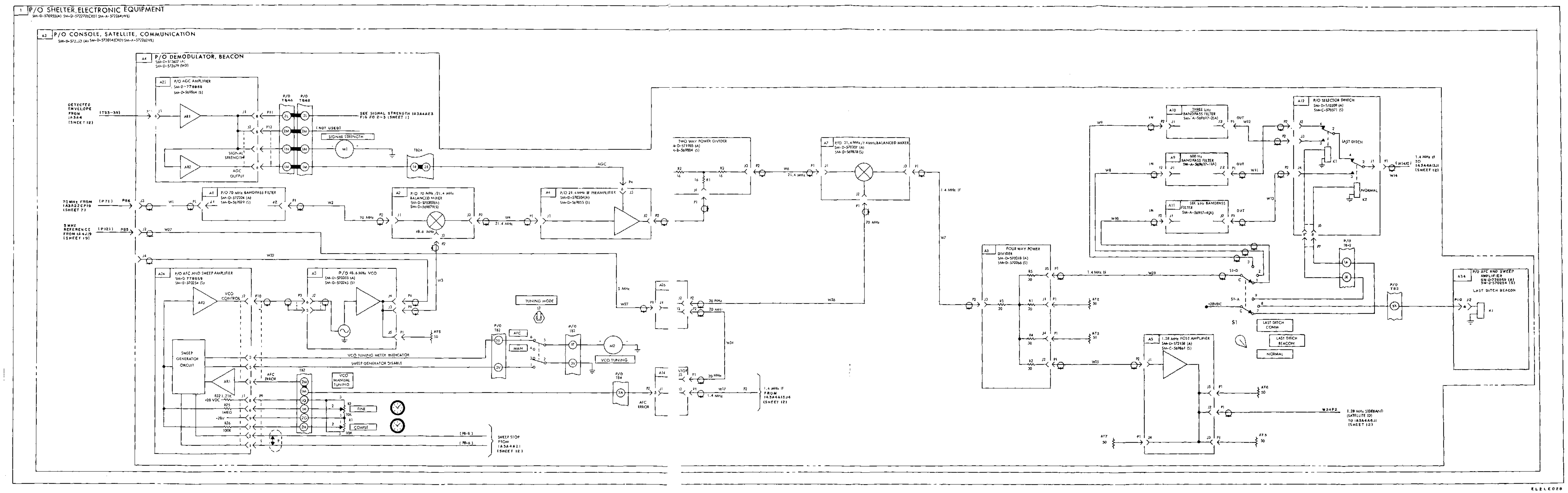

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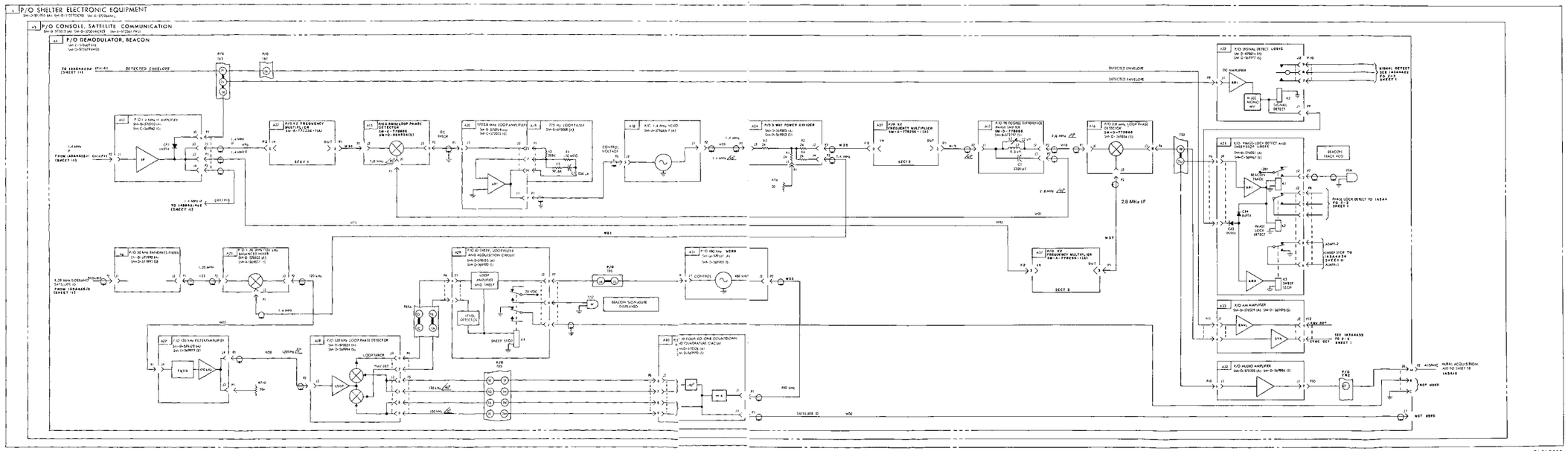

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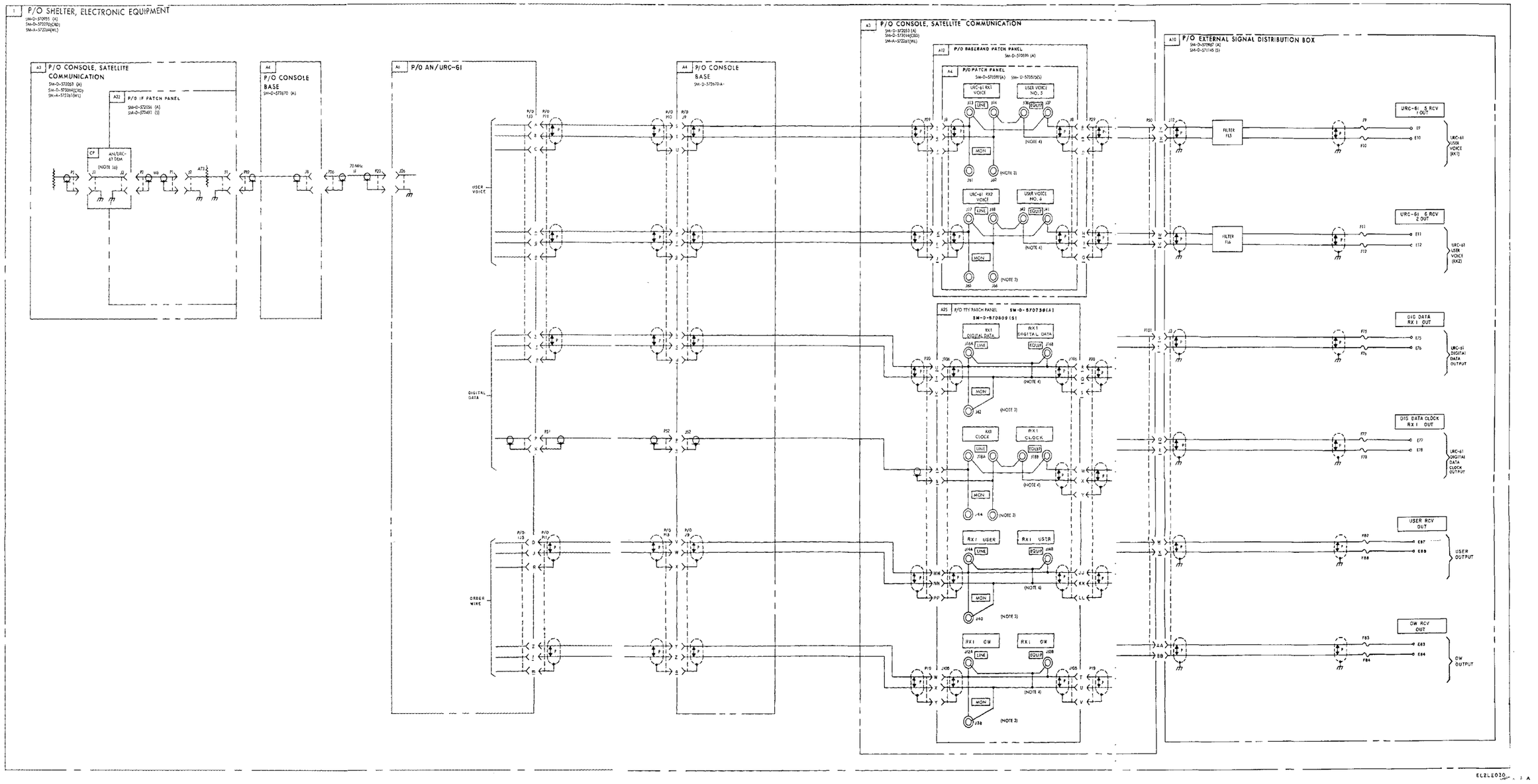

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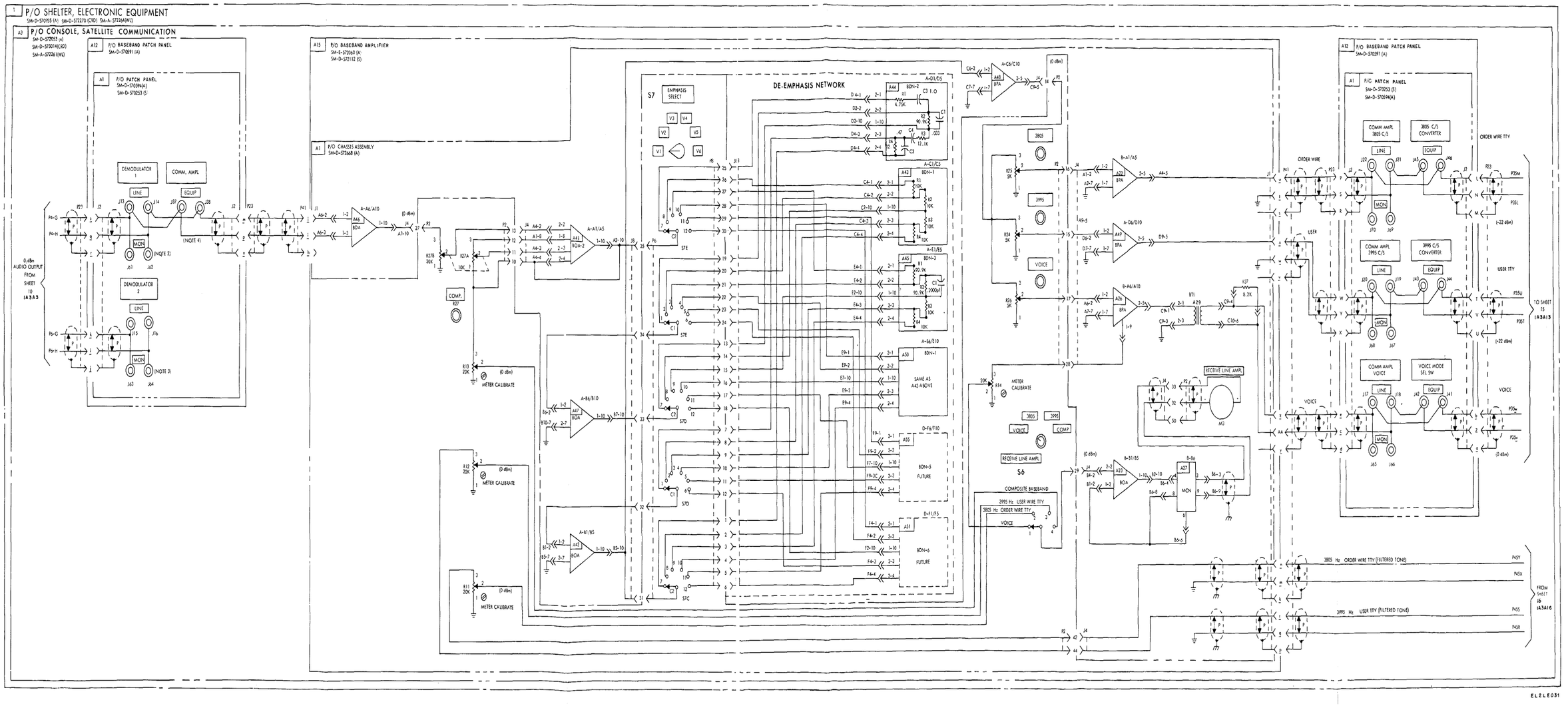

Figure FO 2-2 (14). Satellite Communication Terminal AN/TSC-54, receiving function, signal flow diagram (sheet 14 of 19)

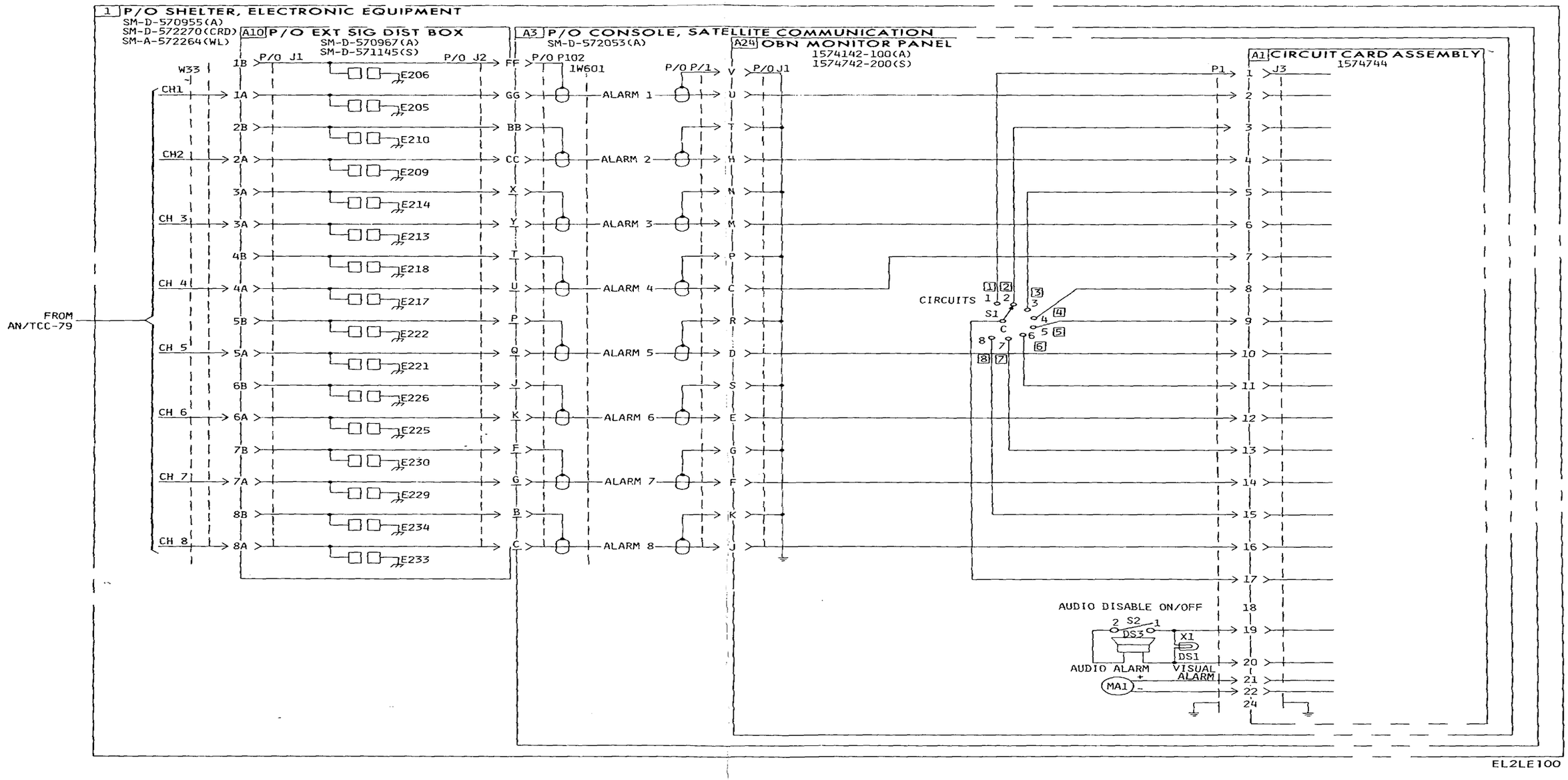

Figure FO 2-2. Satellite Communication Terminal AN/TSC-54, receiving function, signal flow diagram (sheet 14.1)

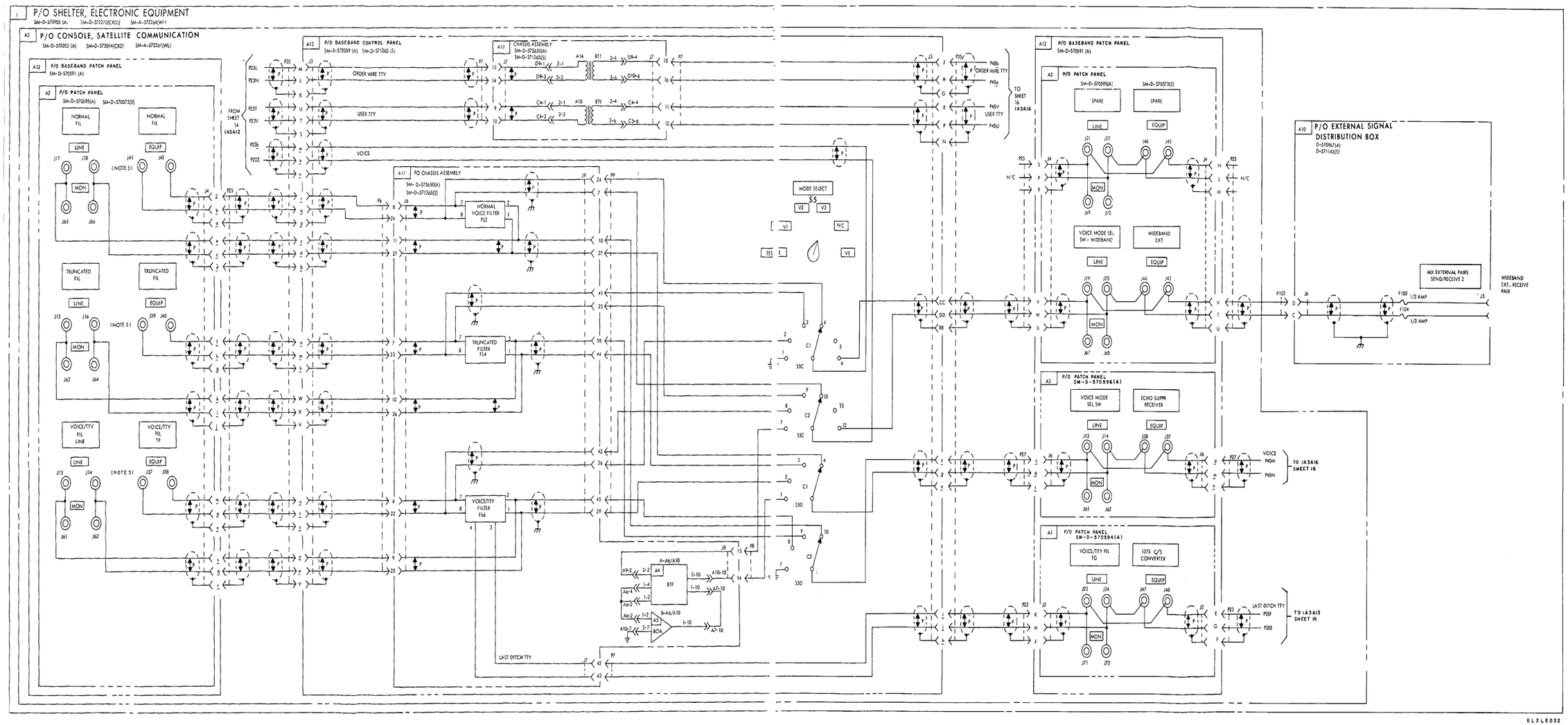

Figure FO 2-2 (15). Satellite Communication Terminal AN/TSC-54, receiving function, signal flow diagram (sheet 15 of 19)

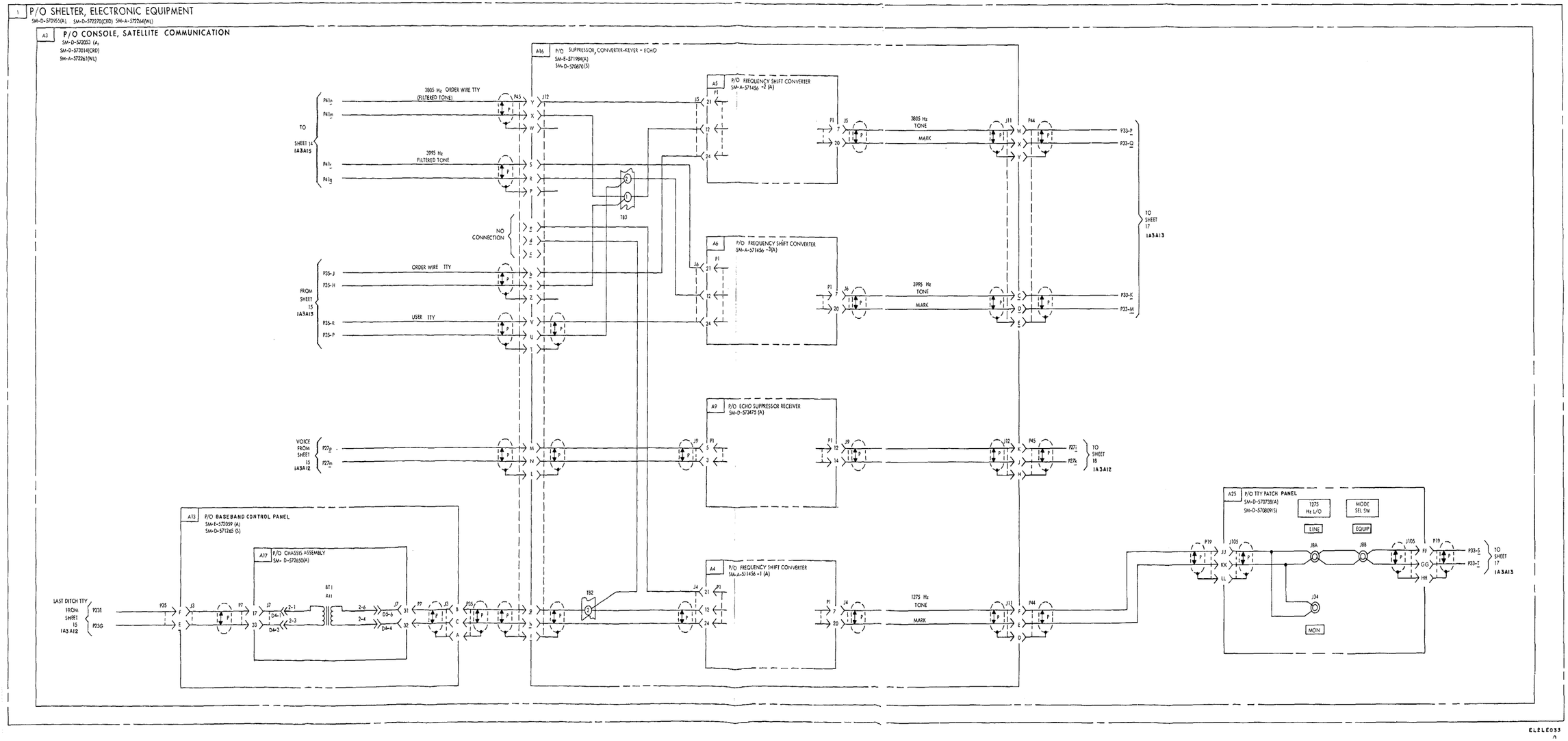

Figure FO 2-2 (16). Satellite Communication Terminal AN/TSC-54, receiving function, signal flow diagram (sheet 16 of 19)

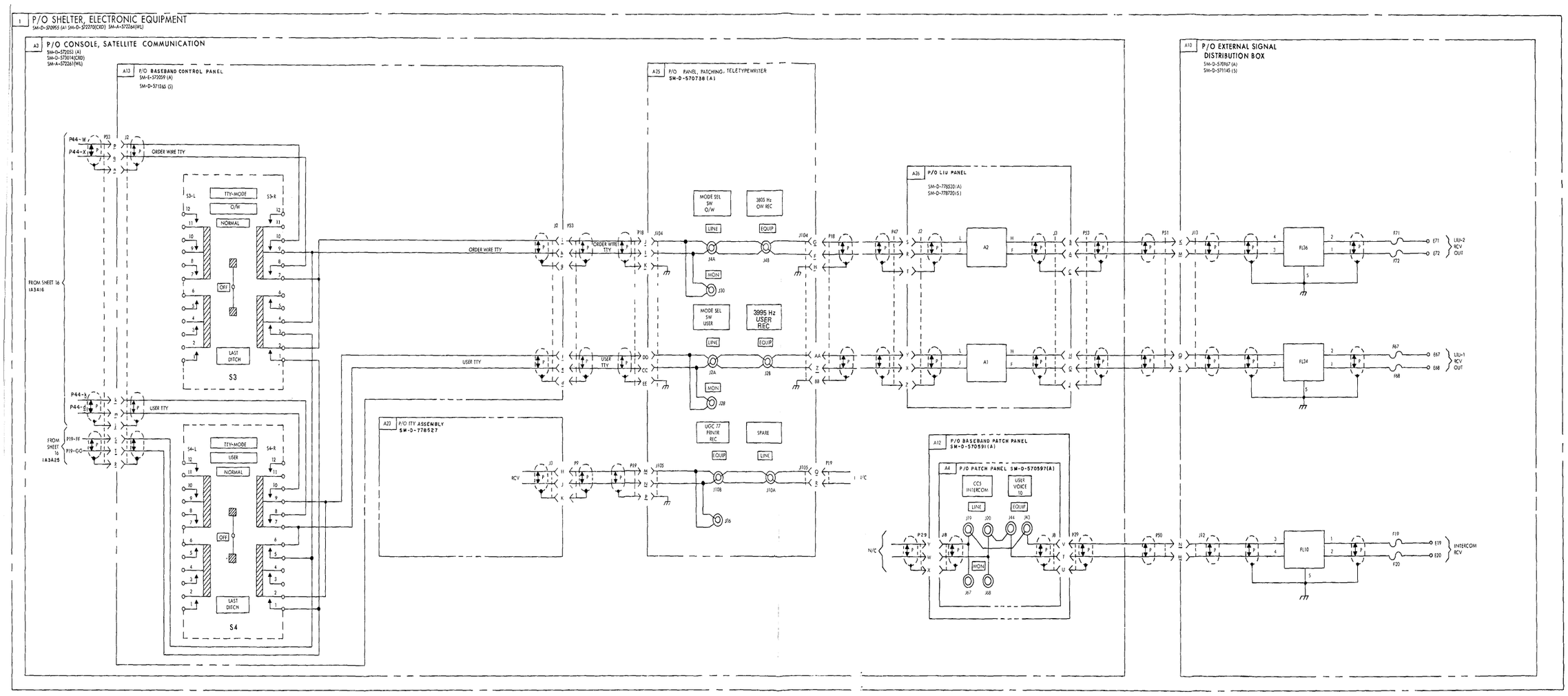

Figure FO 2-2 (17). Satellite Communication Terminal AN/TSC-54, receiving function, signal flow diagram (sheet 17 of 19)

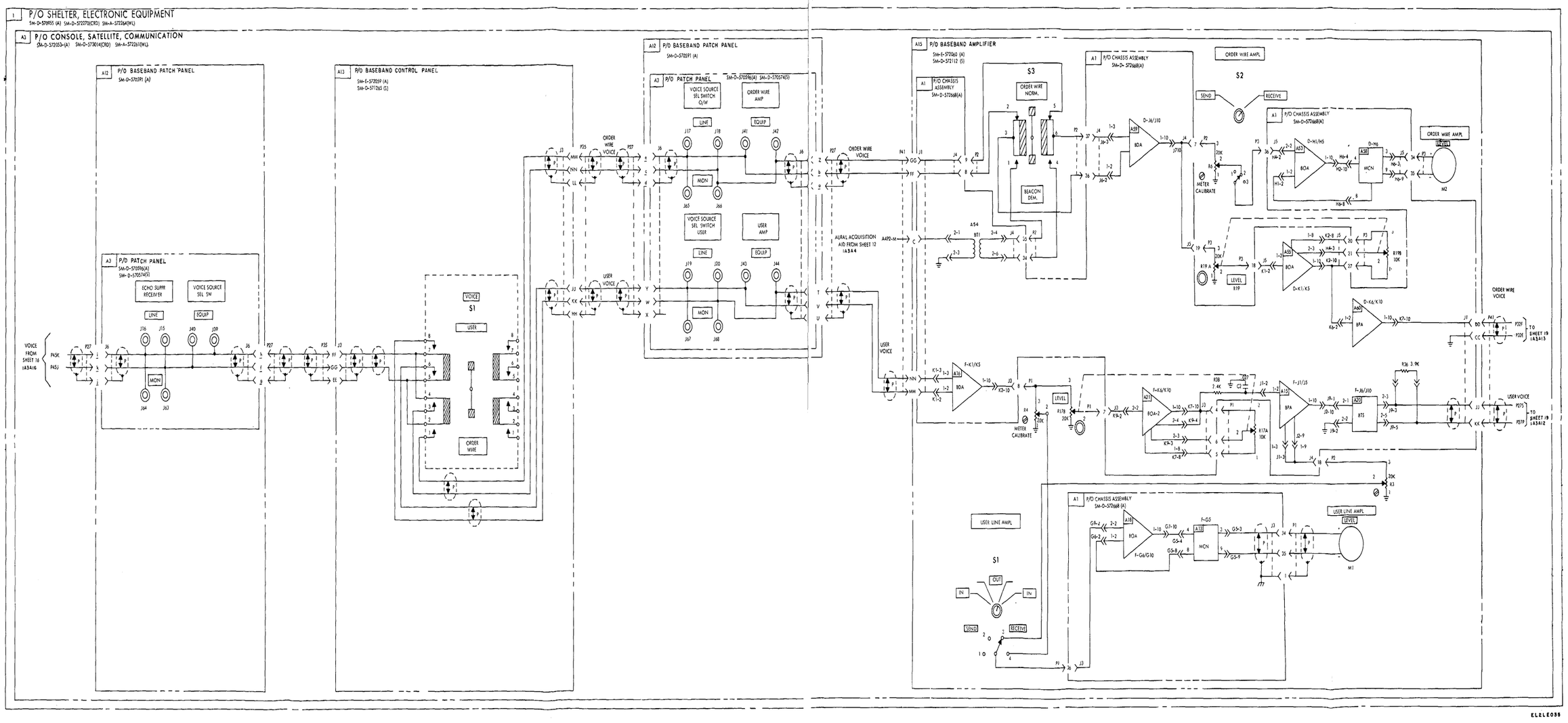

Figure FO 2-2 (18). Satellite Communication Terminal AN/TSC -54, receiving function, signal flow diagram (sheet 18 of 19)

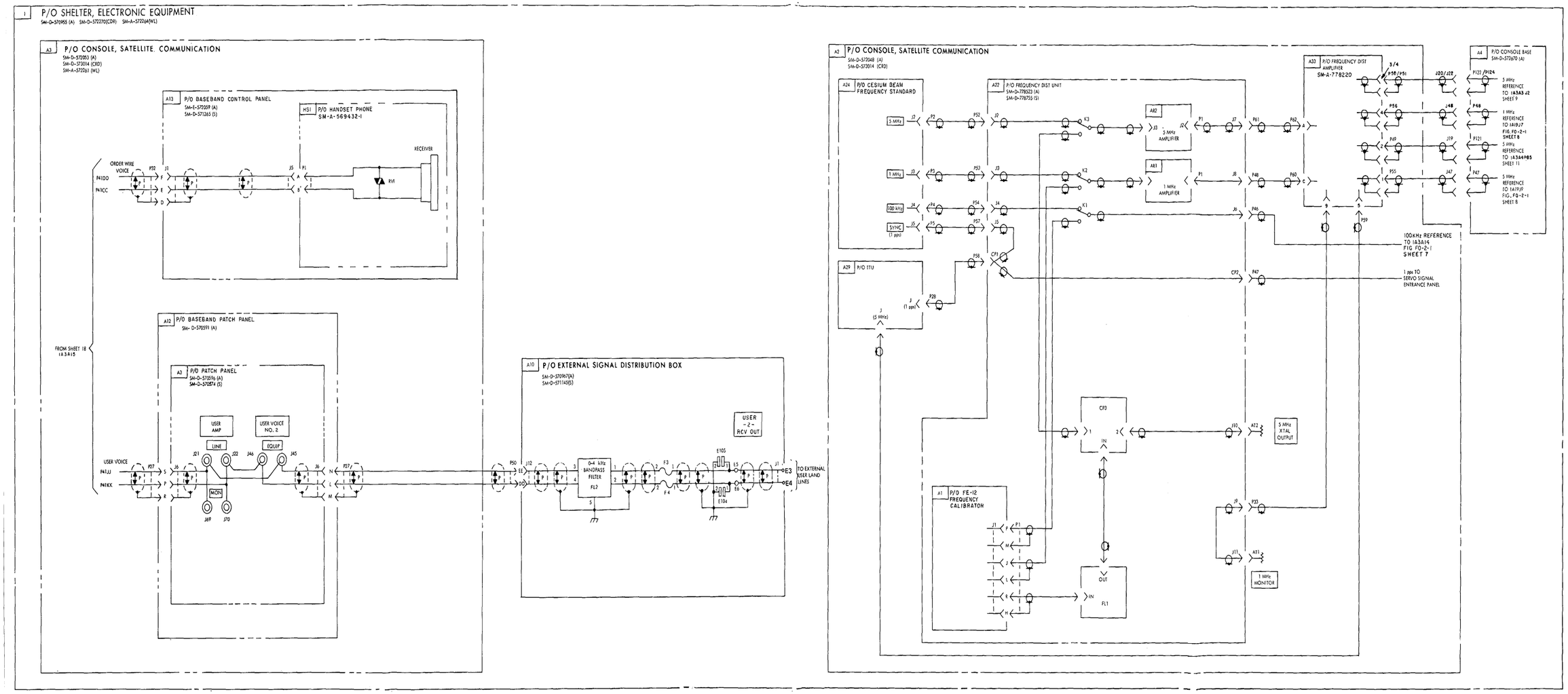

Figure FO 2-2 (19). Satellite Communication Terminal AN/TSC -54, receiving function, signal flow diagram (sheet 19 of 19)

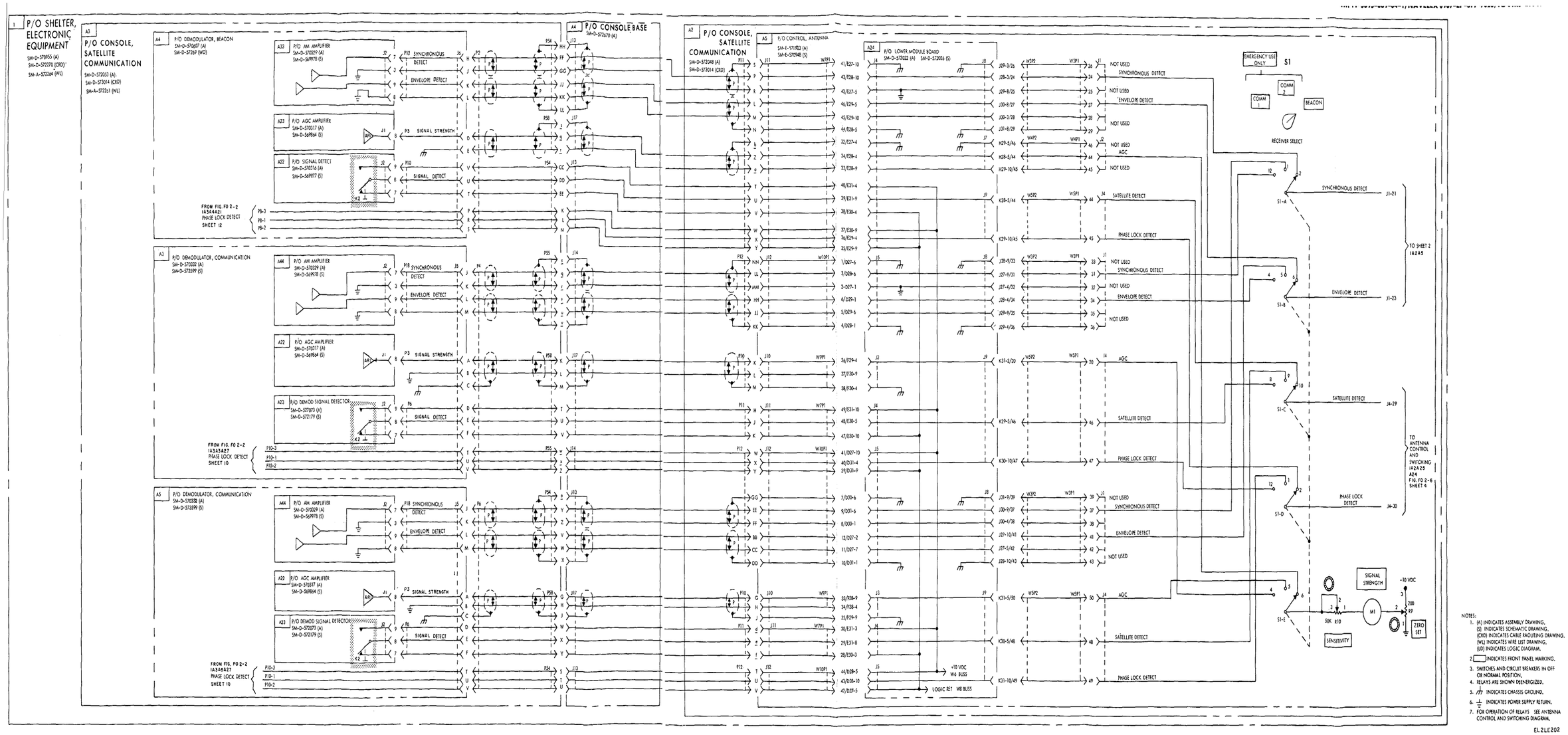

Figure FO 2-3. Satellite Communication Terminal AN/TSC -54, antenna control function, signal flow diagram (sheet 1 of 9)

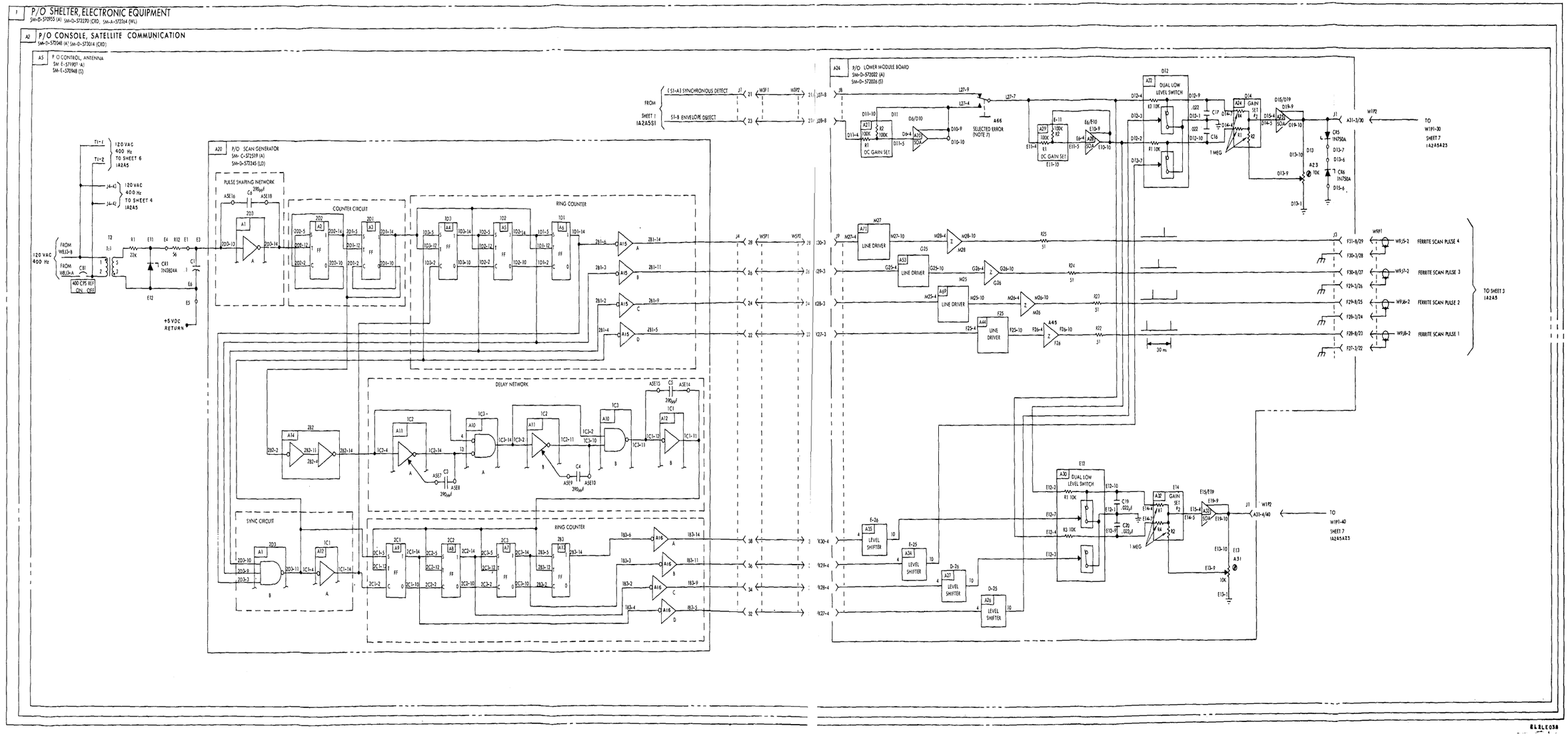

Figure FO 2-3 (2). Satellite Communication Terminal AN/TSC -54, antenna control function, signal flow diagram (sheet 2 of 9)

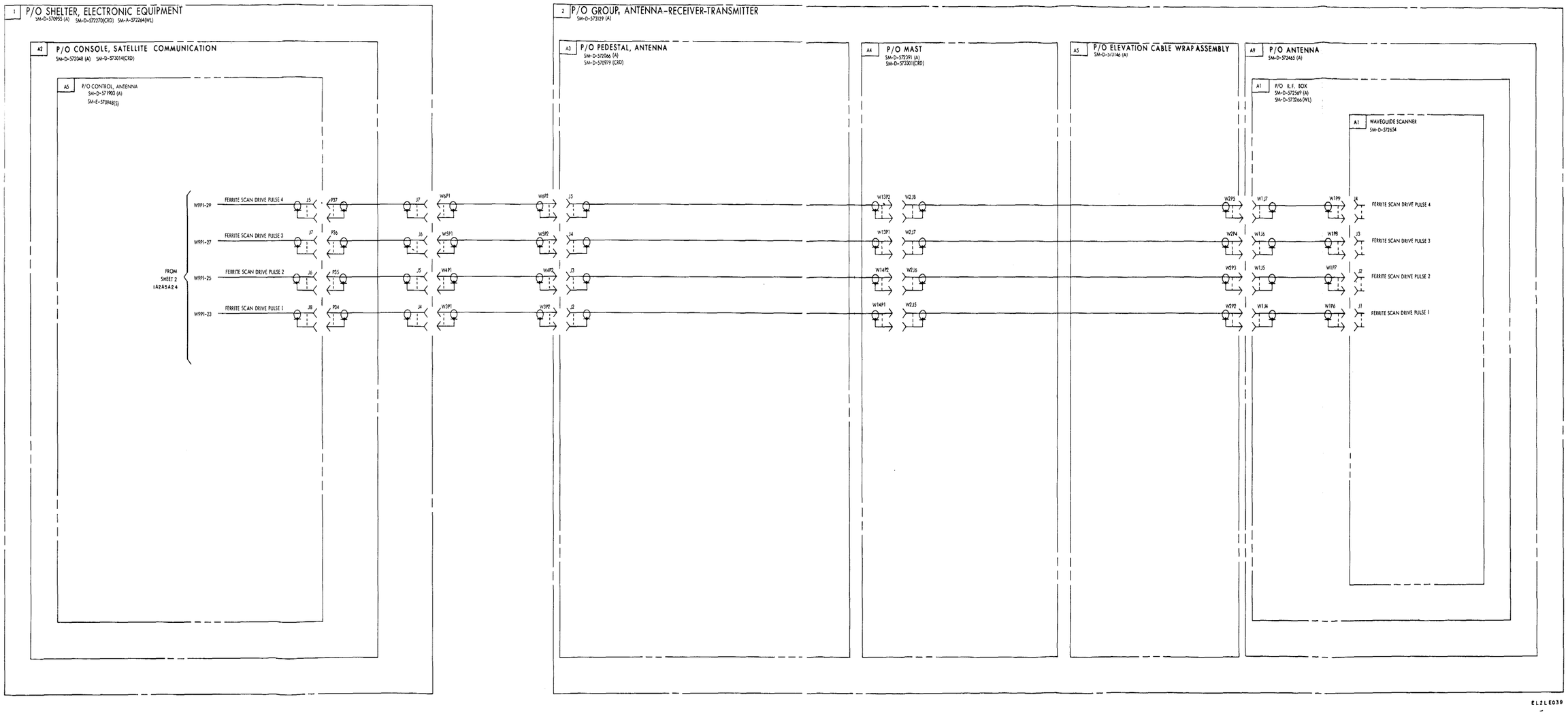

Figure FO 2-3 (3). Satellite Communication Terminal AN/TSC-54, antenna control function, signal flow diagram (sheet 3 of 9)

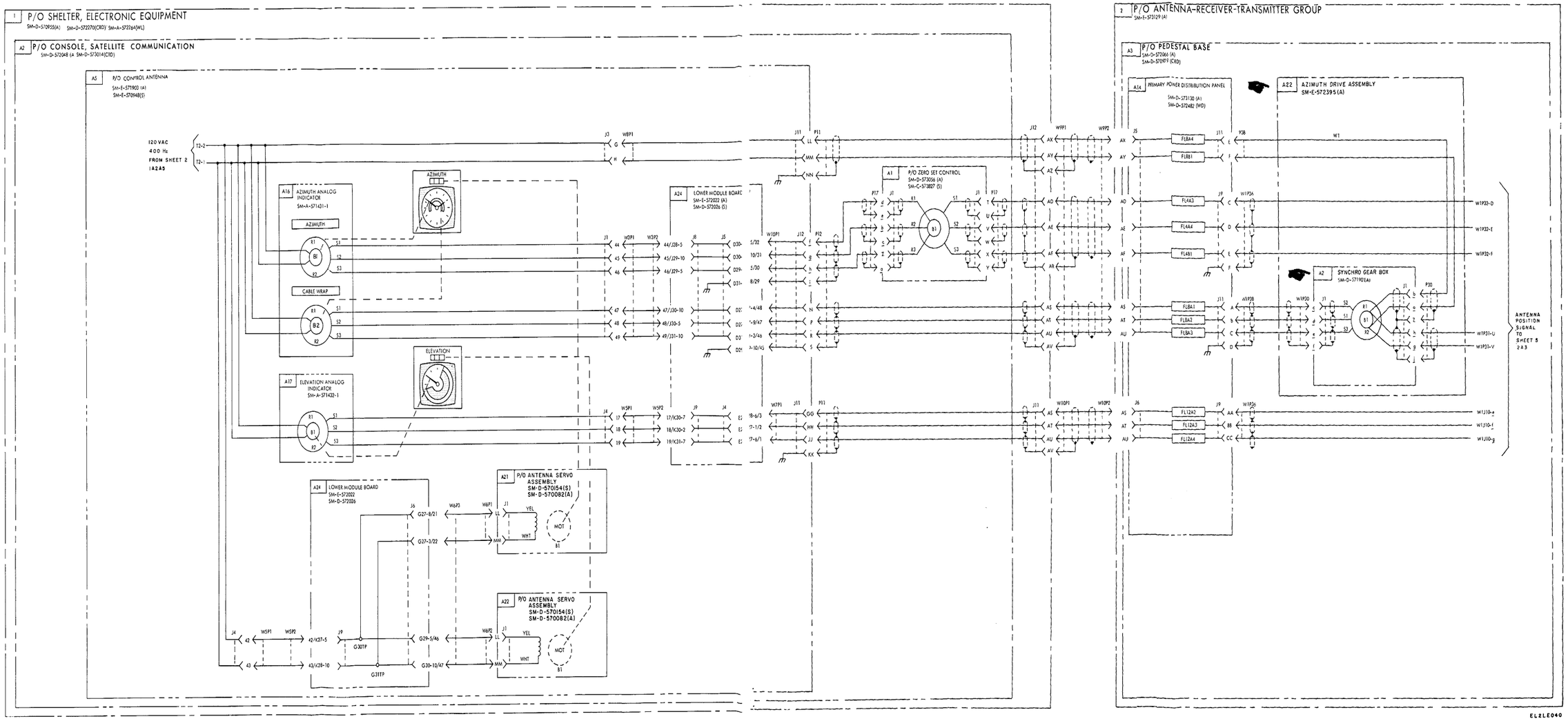

Figure FO 2-3 (4). Satellite Communication Terminal AN/TSC-54, receiving function, signal flow diagram (sheet 4 of 9)

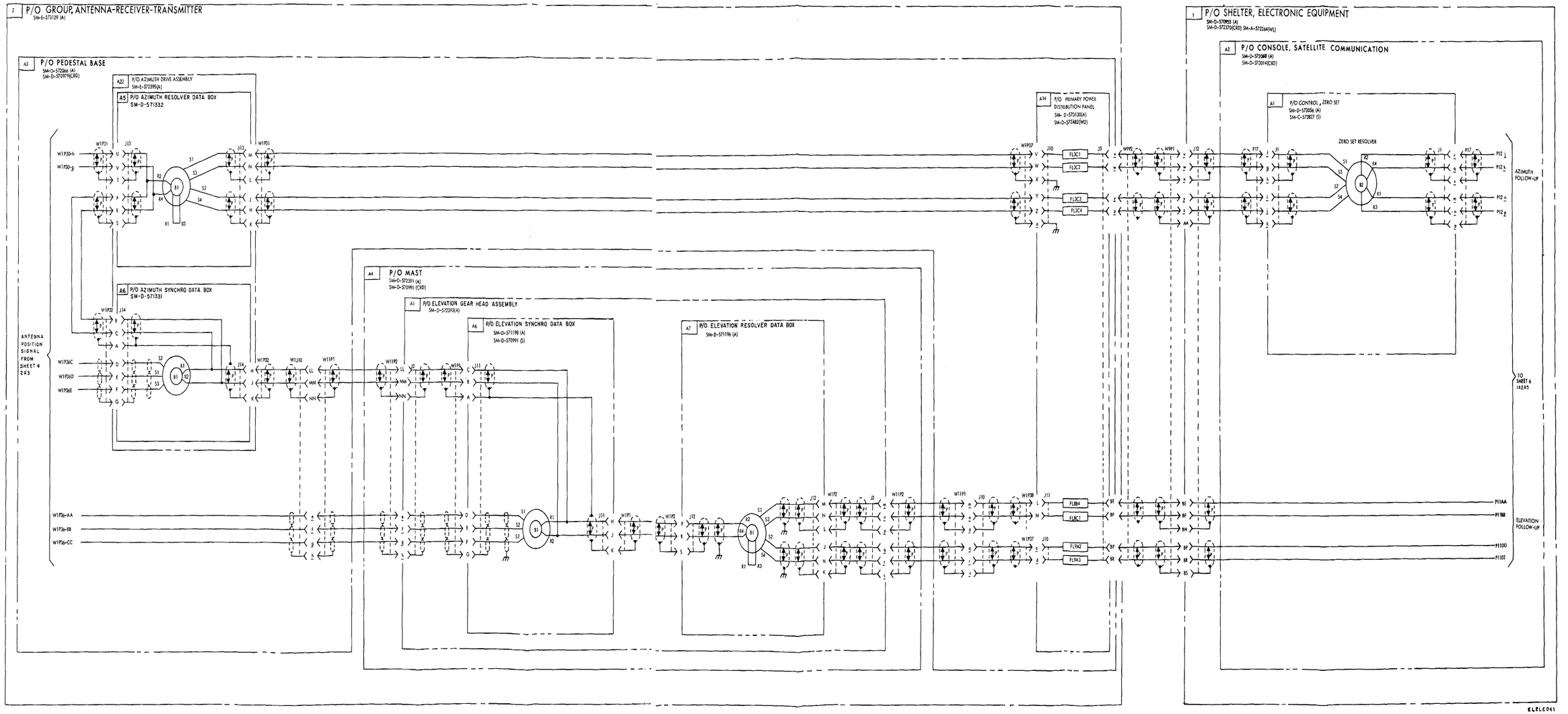

Figure FO 2-3 (5). Satellite Communication Terminal AN/TSC -54, antenna control function, signal flow diagram (sheet 5 of 9)

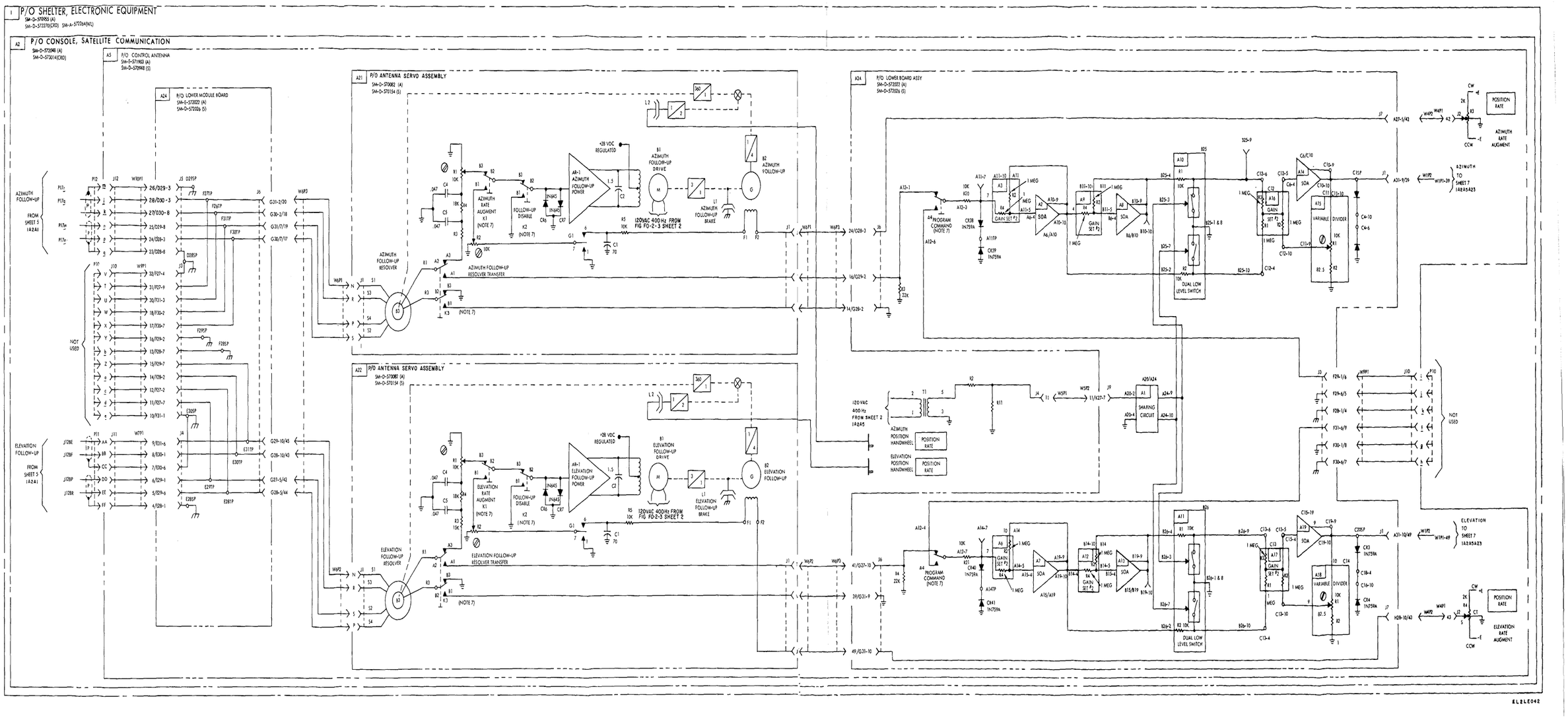

Figure FO 2-3 (6). Satellite Communication Terminal AN/TSC -54, antenna control function, signal flow diagram (sheet 6 of 9)

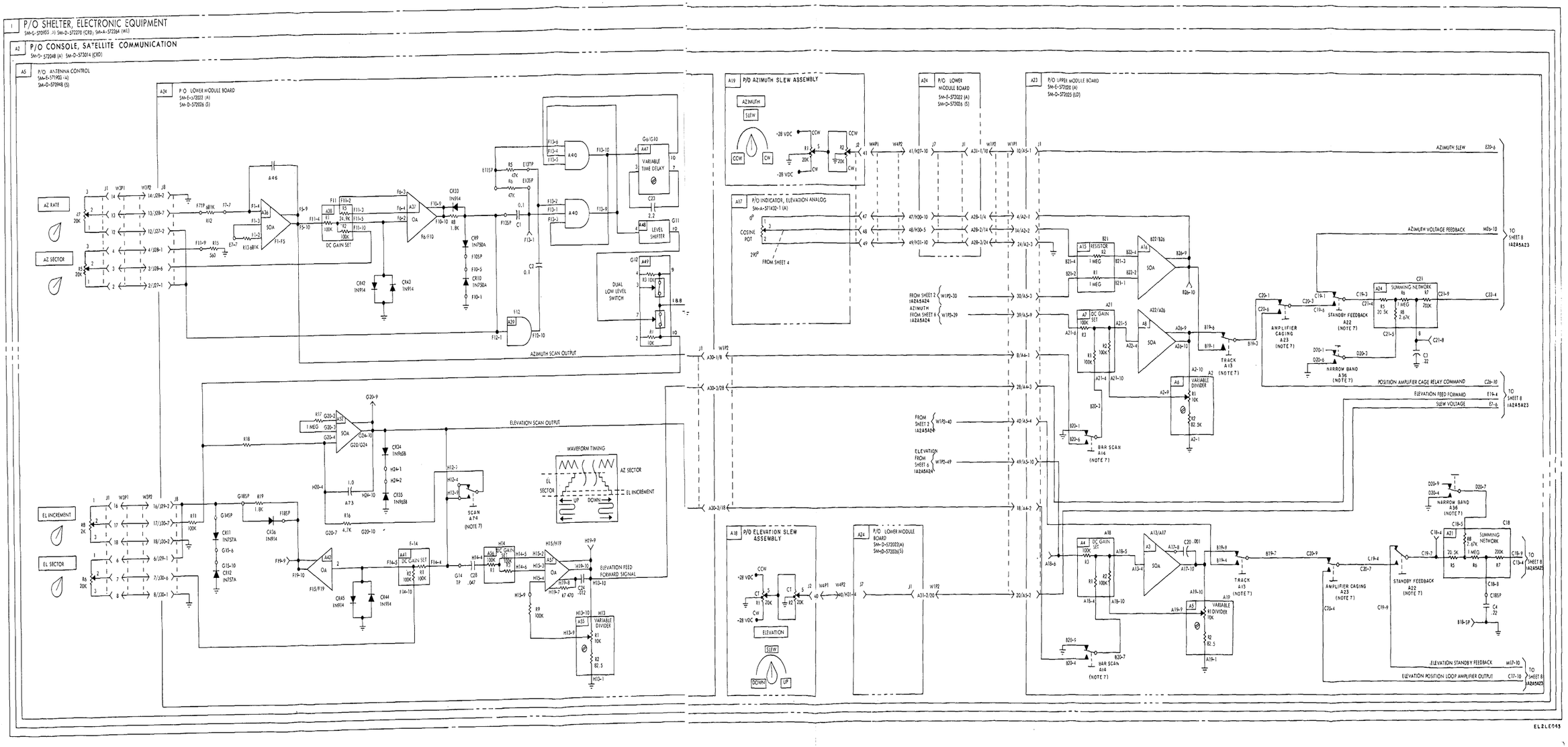

Figure FO 2-3 (7). Satellite Communication Terminal AN/TSC -54, antenna control function, signal flow diagram (sheet 7 of 9)

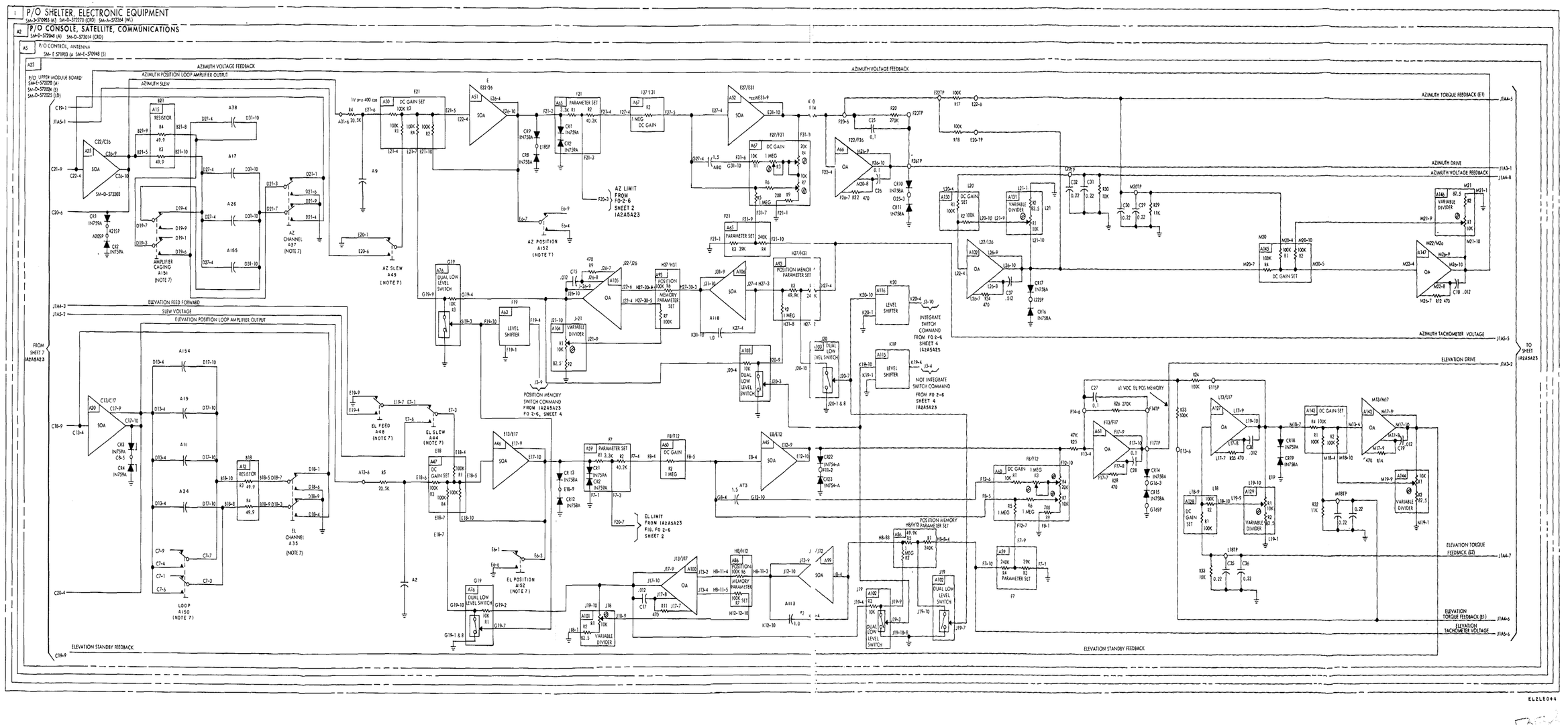

Figure FO 2-3 (8). Satellite Communication Terminal AN/TSC -54, antenna control function, signal flow diagram (sheet 8 of 9)

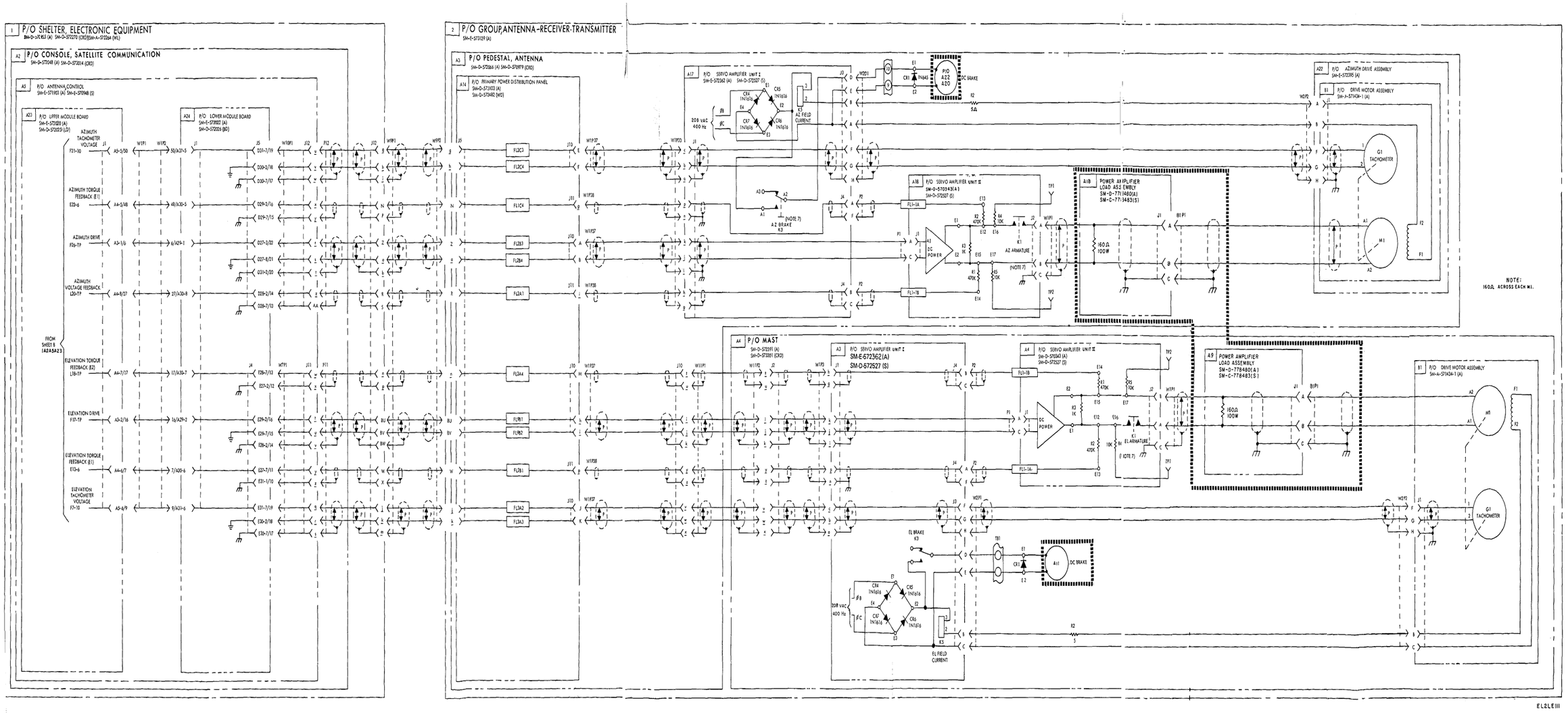

Figure FO 2-3 . Satellite Communication Terminal AN/TSC -54, antenna control function, signal flow diagram (sheet 9 of 9)

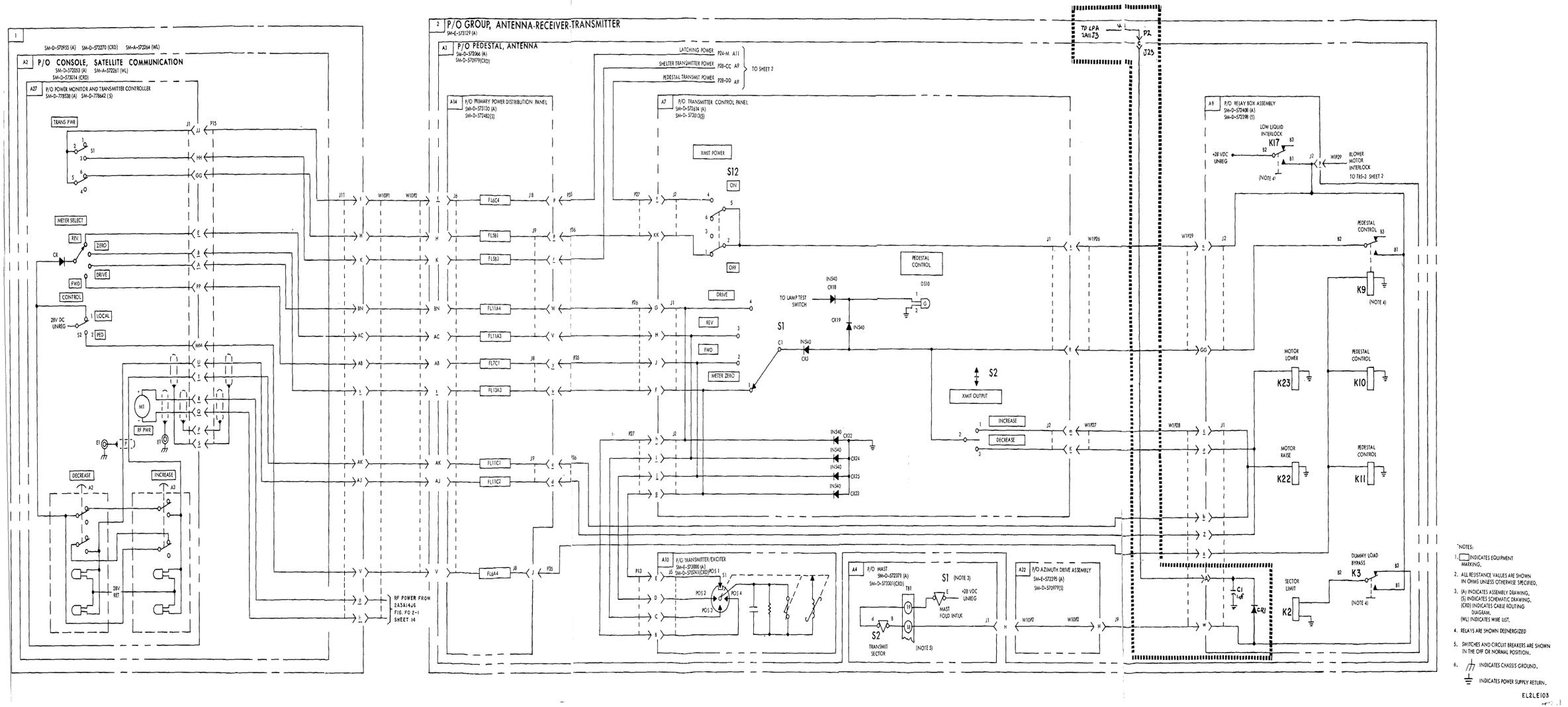

Figure FO- 2-4 . Satellite Communication Terminal AN/TSC -54, receiving function, signal flow diagram (sheet 1 of 7).

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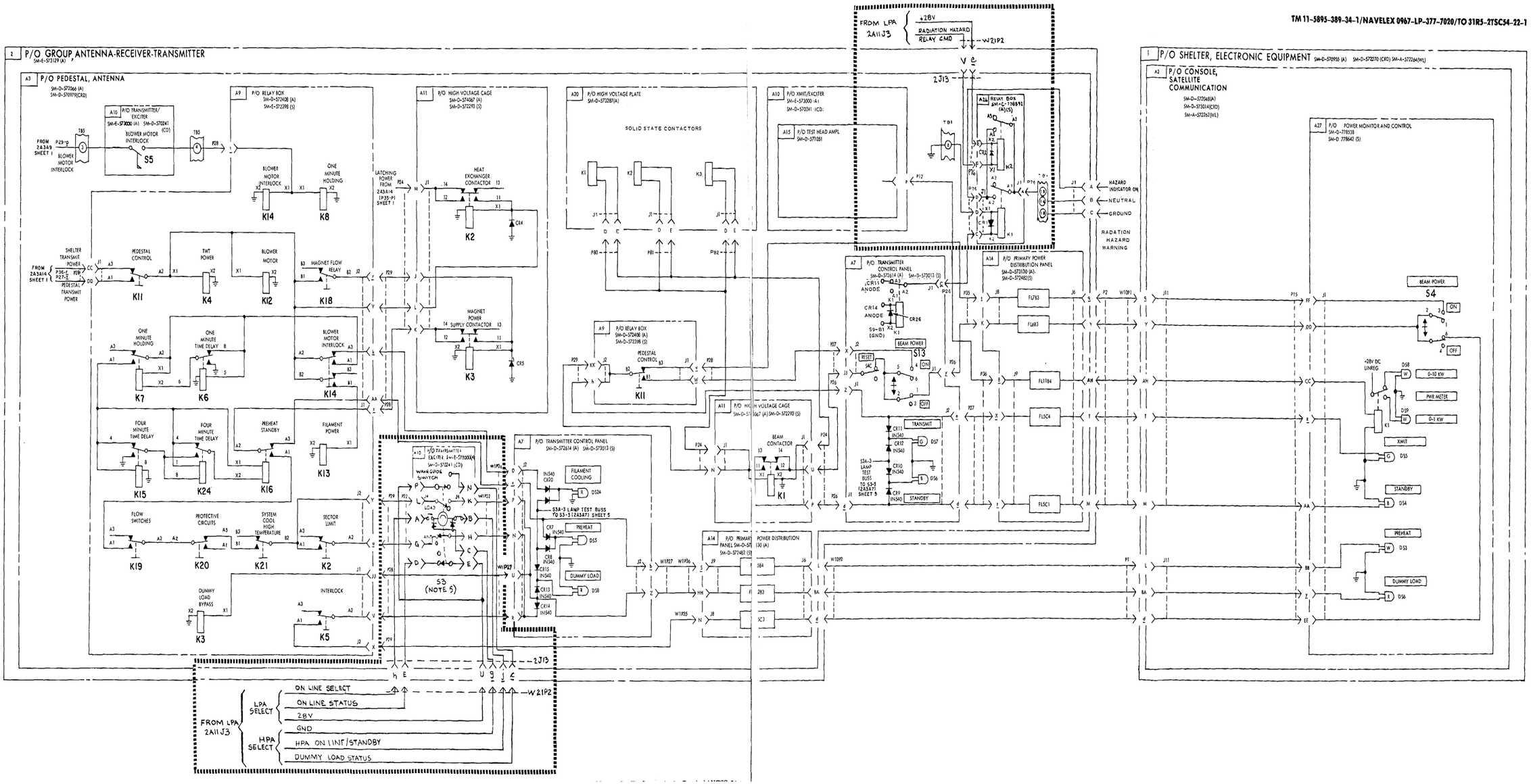

Figure FO 2-4 . Satellite Communication Terminal AN/TSC -54, transmitting control and switching diagram (sheet 2 of 7)

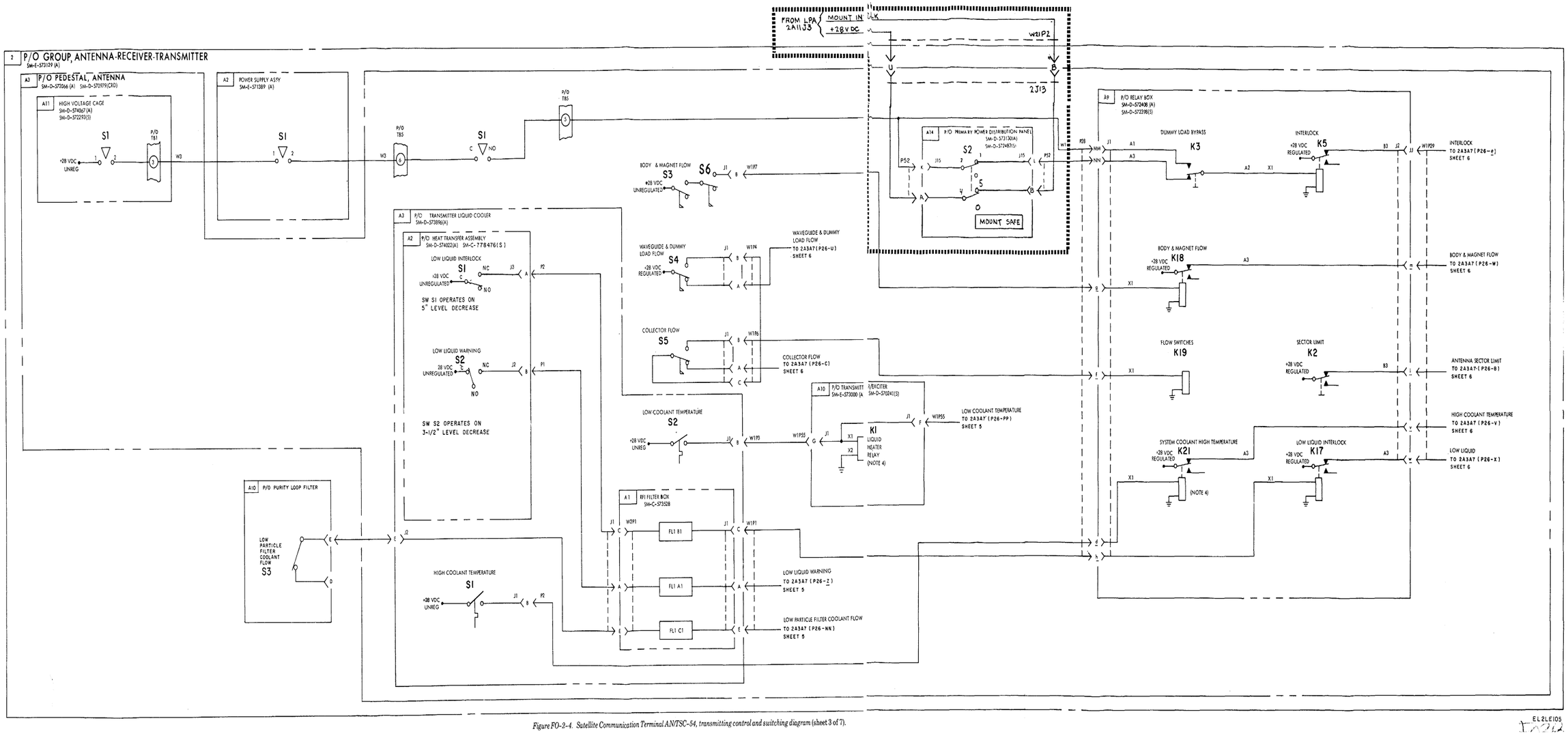

Figure FO-2-4. Satellite Communication Terminal AN/TSC-54, transmitting control and switching diagram (sheet 3 of 7).

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Figure FO 2-4. Satellite Communication Terminal AN/TSC -54, transmitting control and switching diagram (sheet 3 of 7)

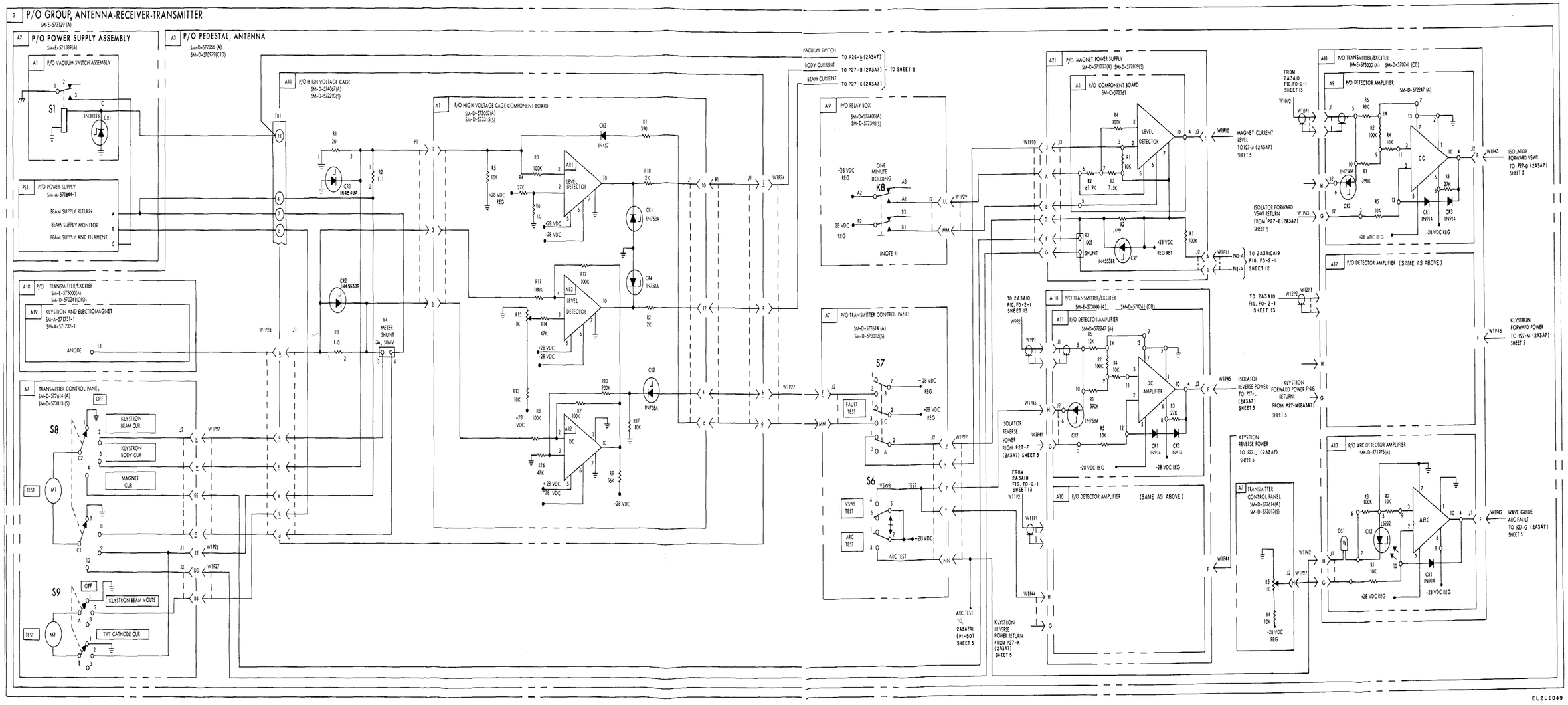

Figure FO 2-4 (4). Satellite Communication Terminal AN/TSC -54, transmitting control and switching diagram (sheet 4 of 7.)

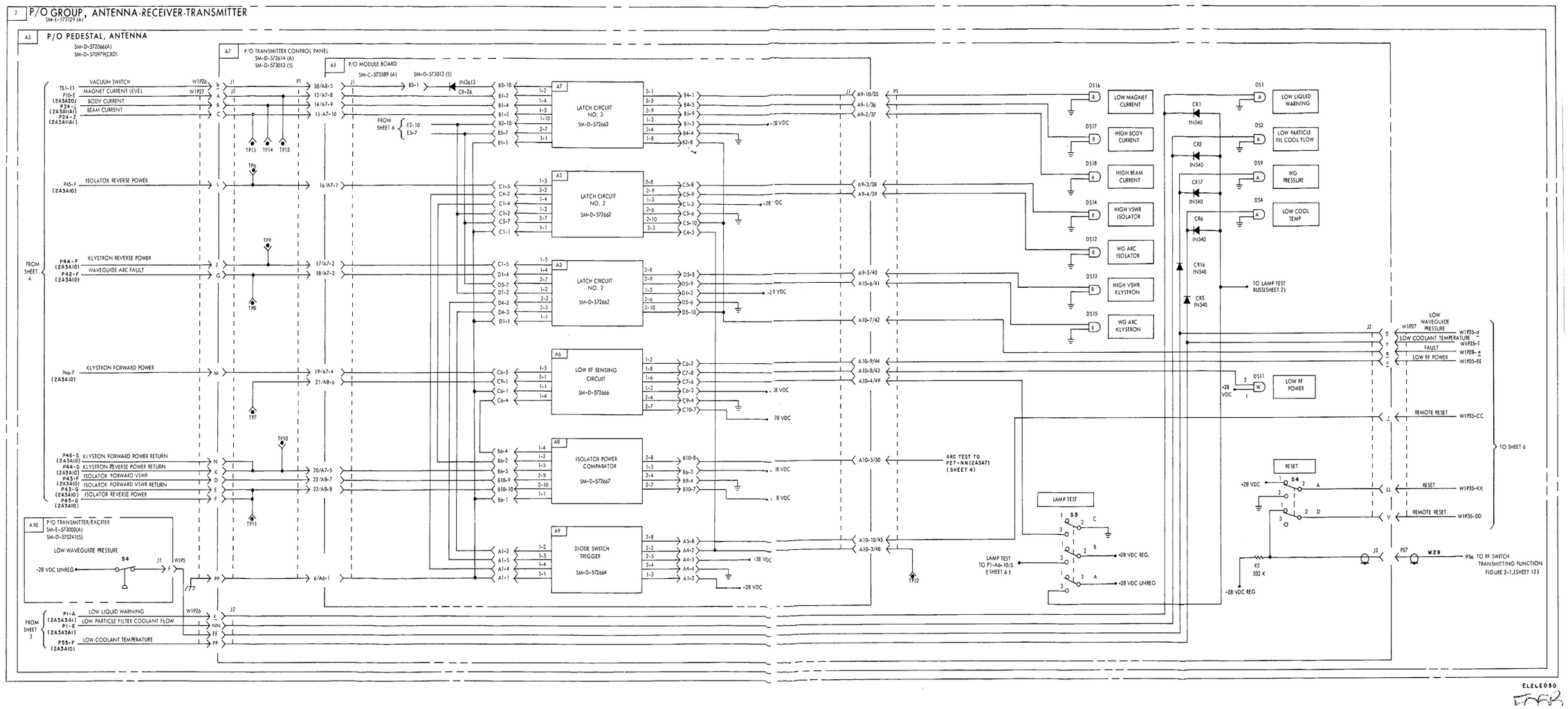

Figure FO 2-4 (5). Satellite Communication Terminal AN/TSC -54, transmitting control and switching diagram (sheet 5 of 7.)

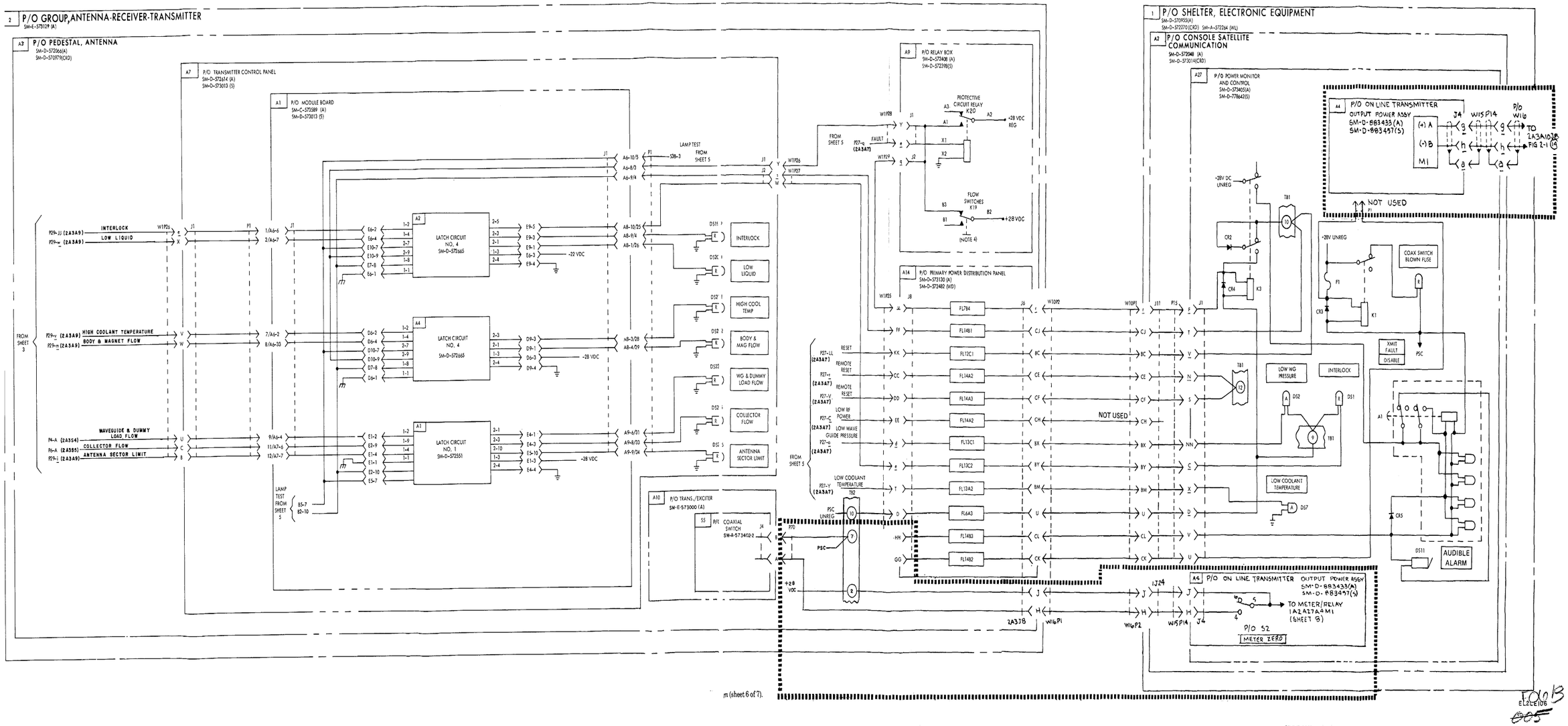

Figure FO 2-4. Satellite Communication Terminal AN/TSC -54, transmitting control and switching diagram (sheet 6 of 7.)

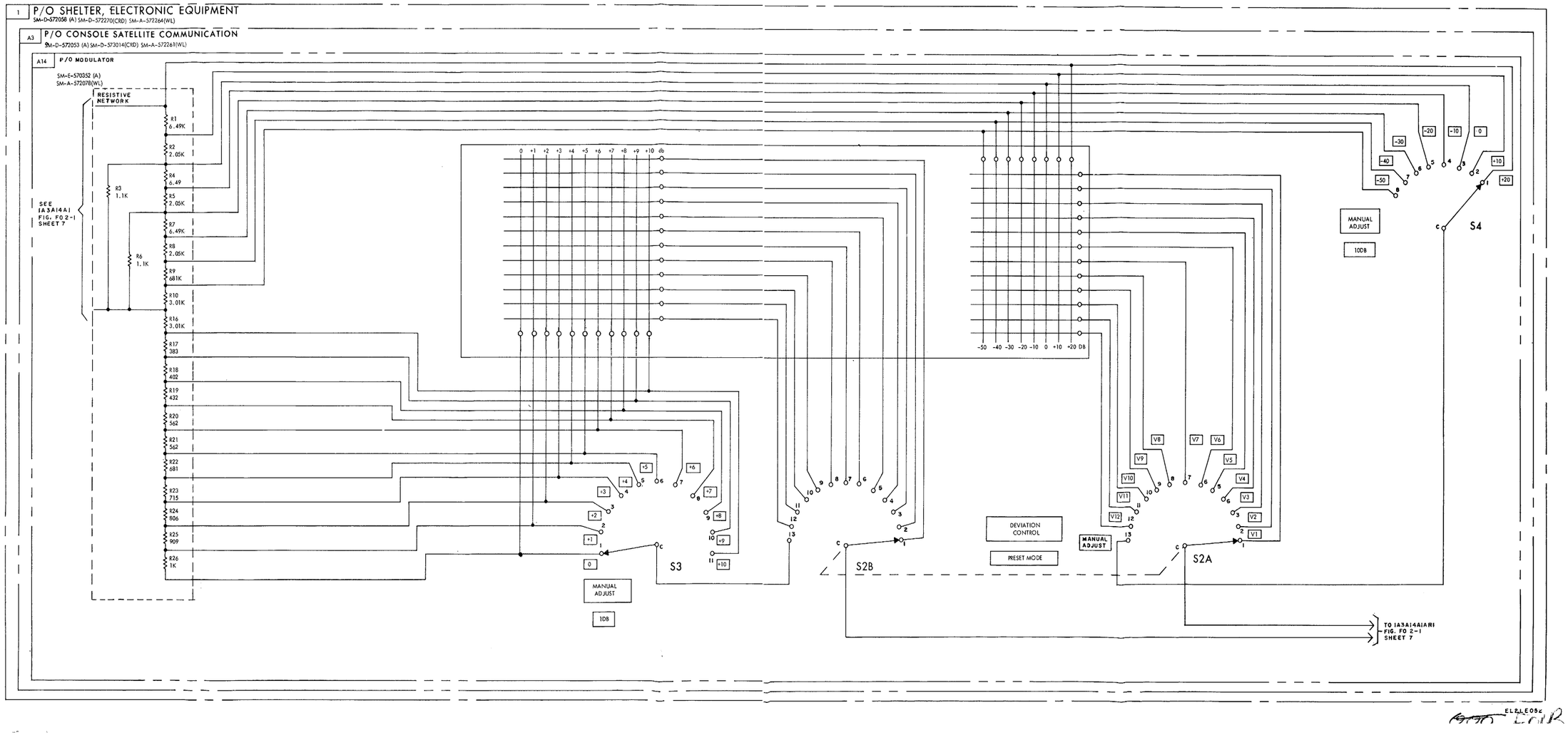

Figure FO 2-4 (7). Satellite Communication Terminal AN/TSC -54, transmitting control and switching diagram (sheet 7 of 7).

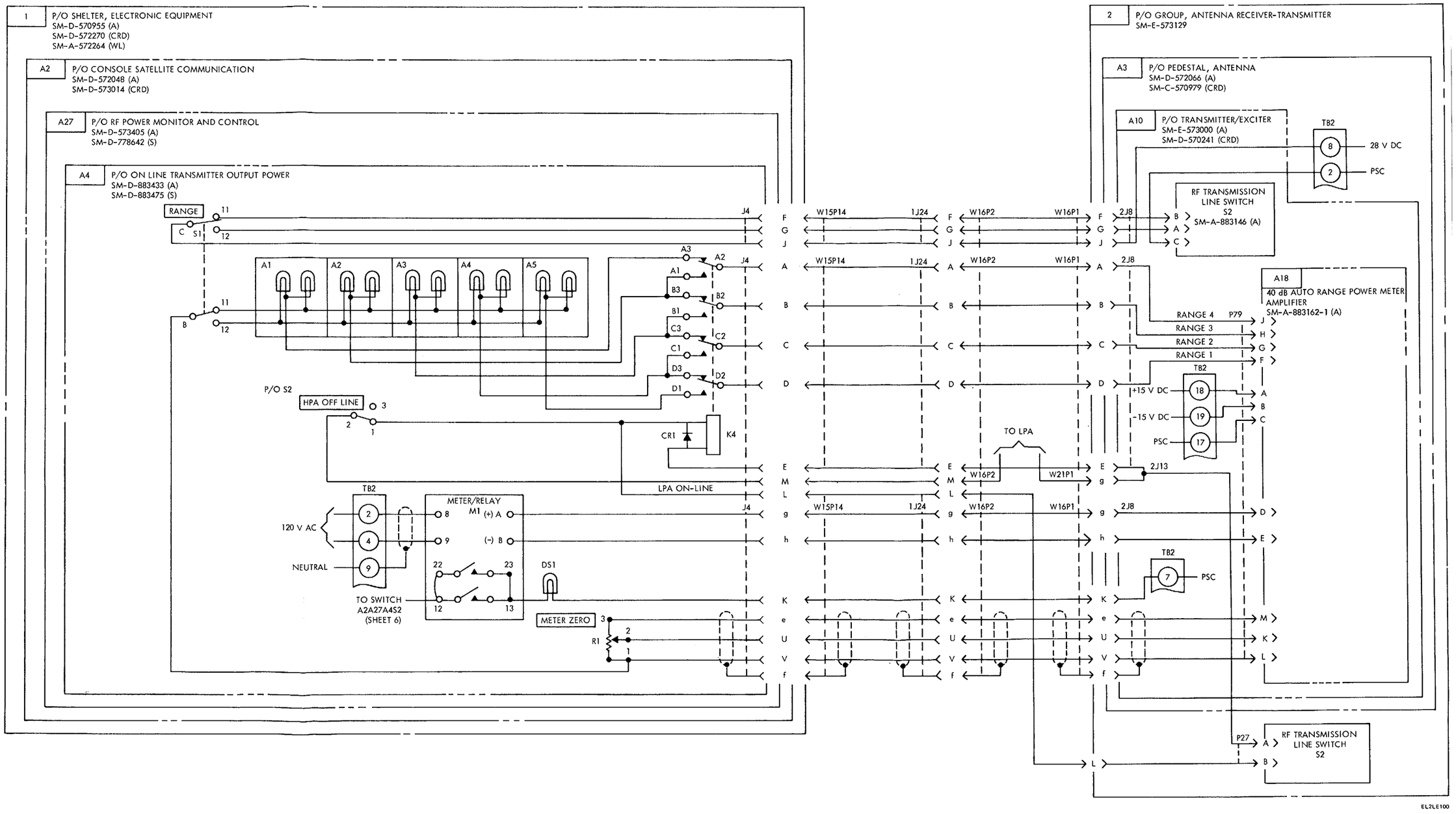

Figure FO 2-4. Satellite Communication Terminal AN/TSC-54, transmitting control and switching diagram (sheet 7.1).

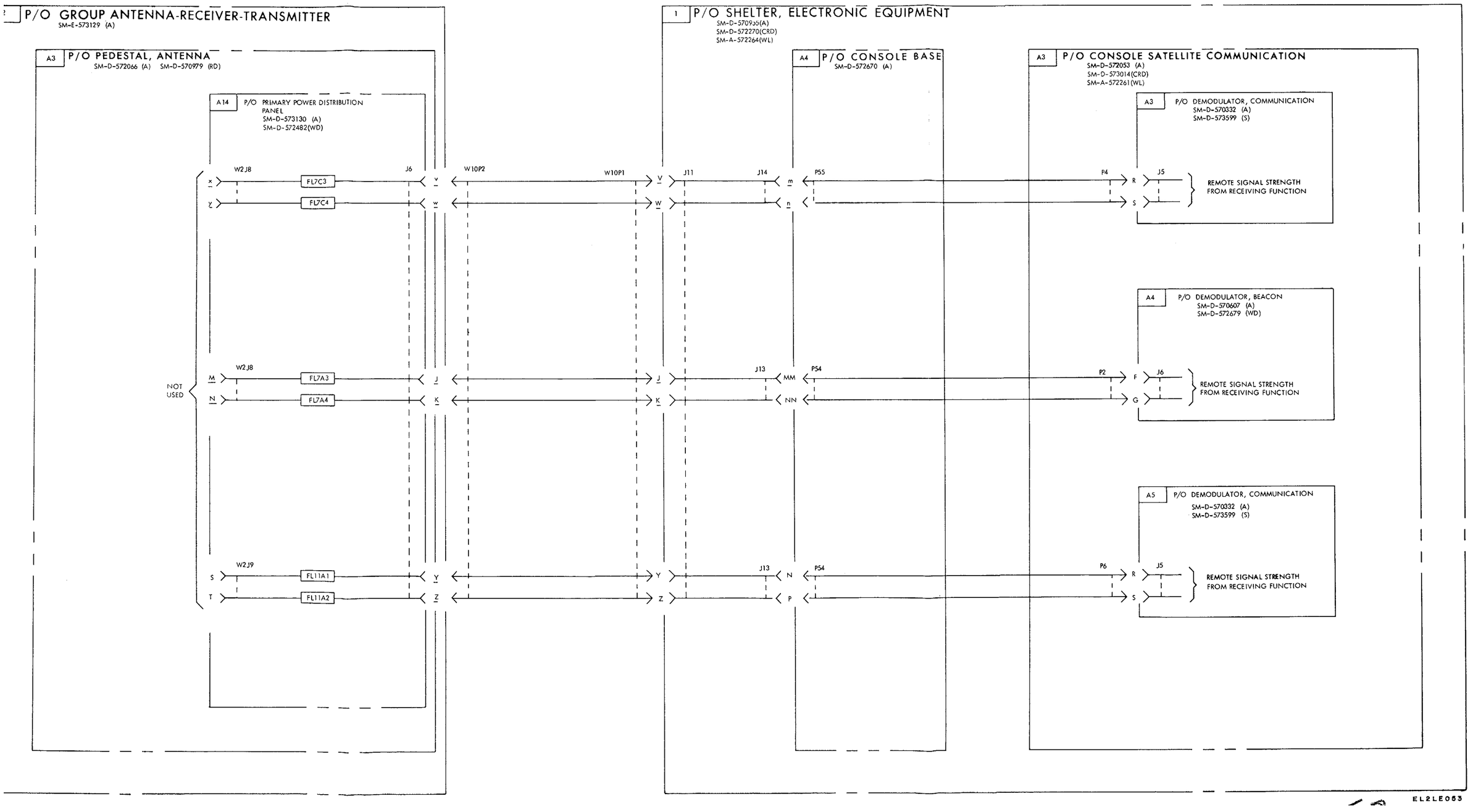

Figure FO 2-5 (1). Satellite Communication Terminal AN/TSC-54, receiving control and switching diagram (sheet 1 of 6).

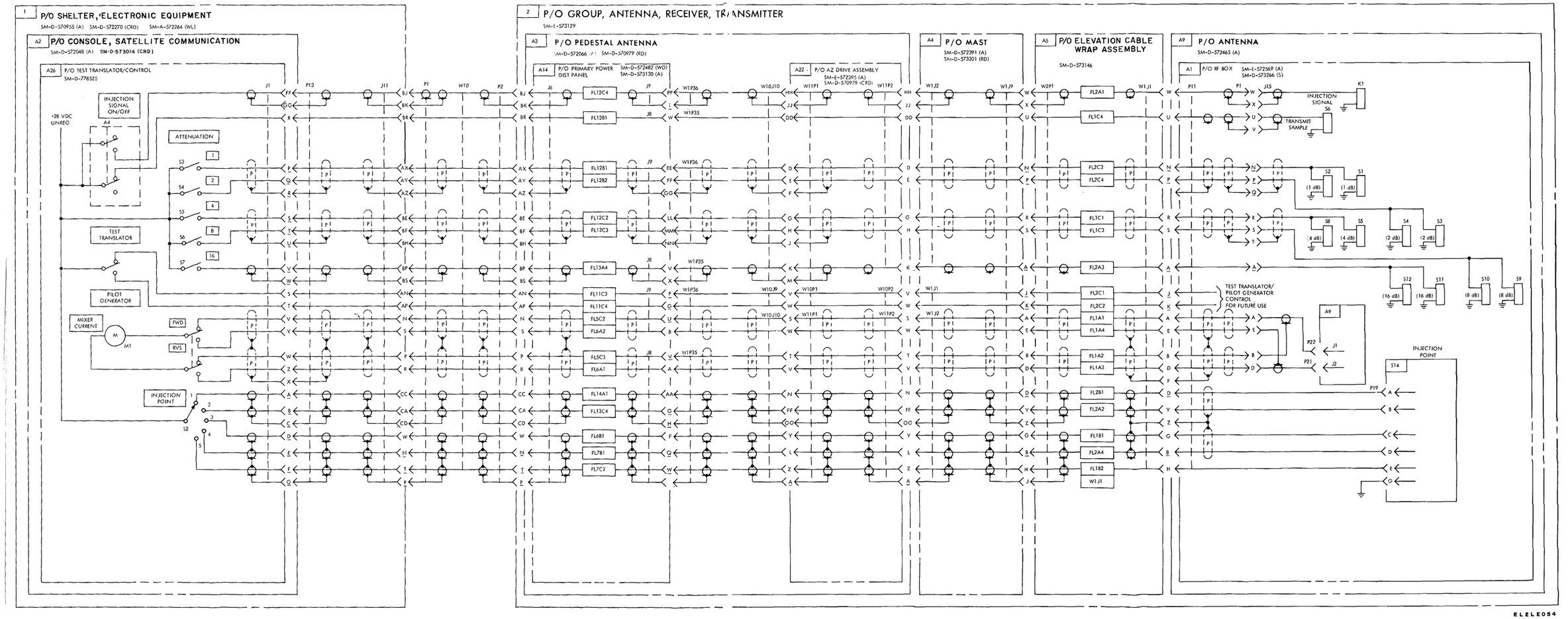

Figure FO 2-5 (2). Satellite Communication Terminal AN/TSC-54, receiving control and switching diagram (sheet 2 of 6).

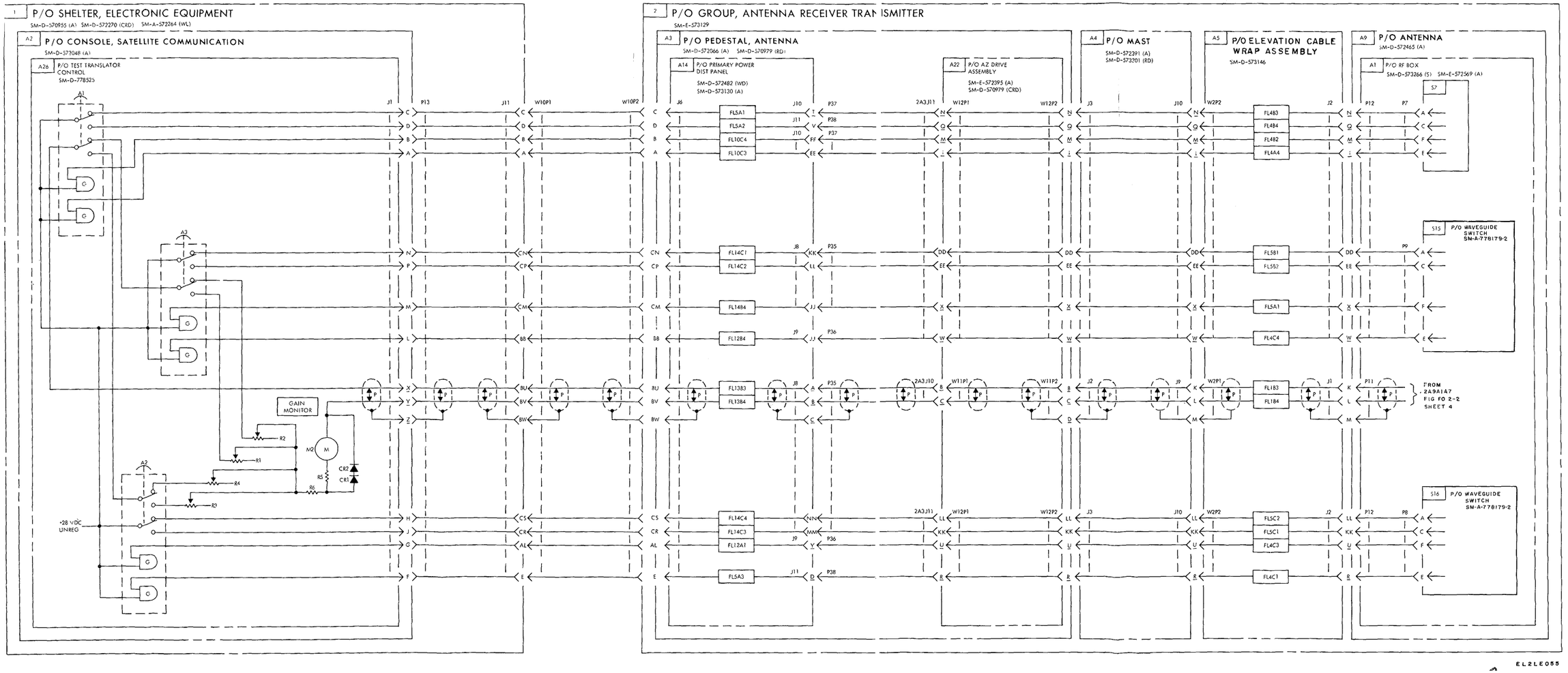

Figure FO 2-5 (3). Satellite Communication Terminal AN/TSC-54, receiving control and switching diagram (sheet 3 of 6).

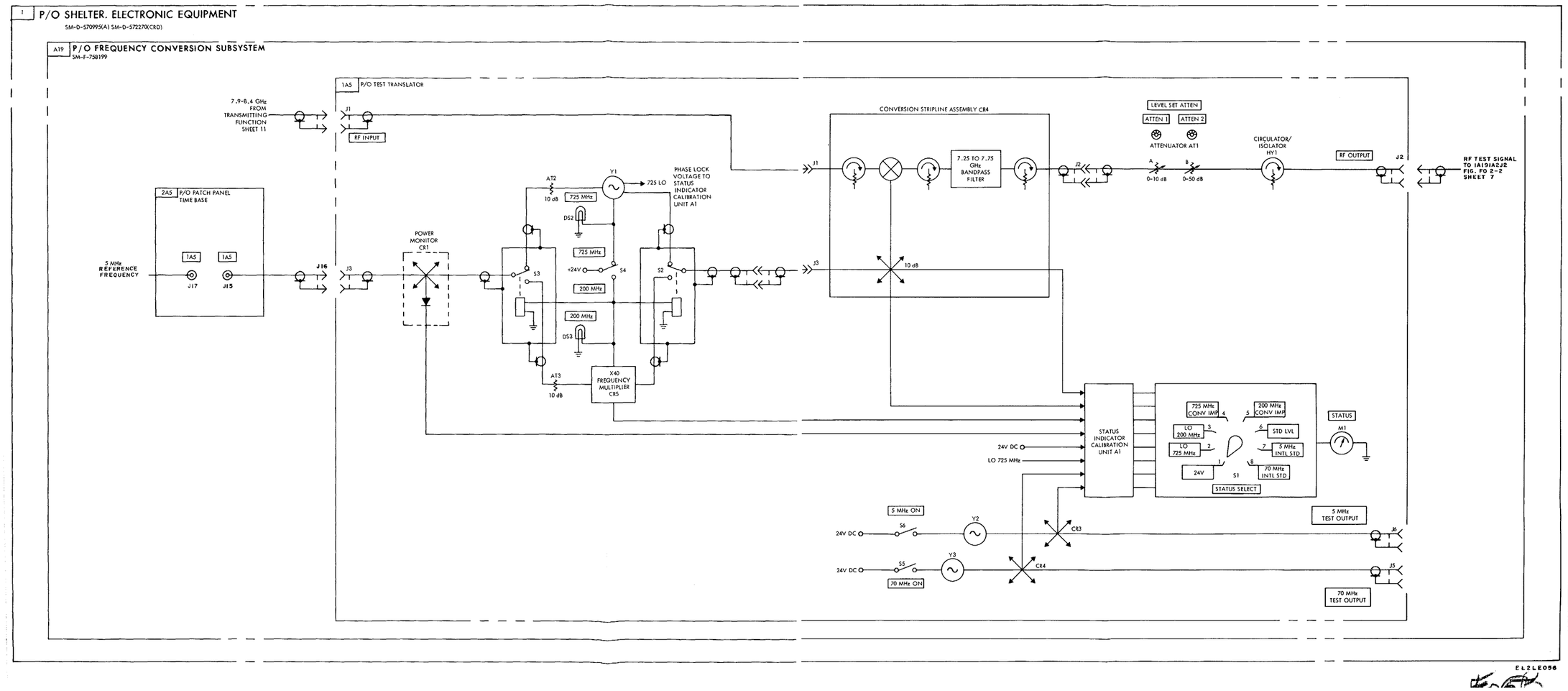

Figure FO 2-5 (4). Satellite Communication Terminal AN/TSC-54, receiving control and switching diagram (sheet 4 of 6).

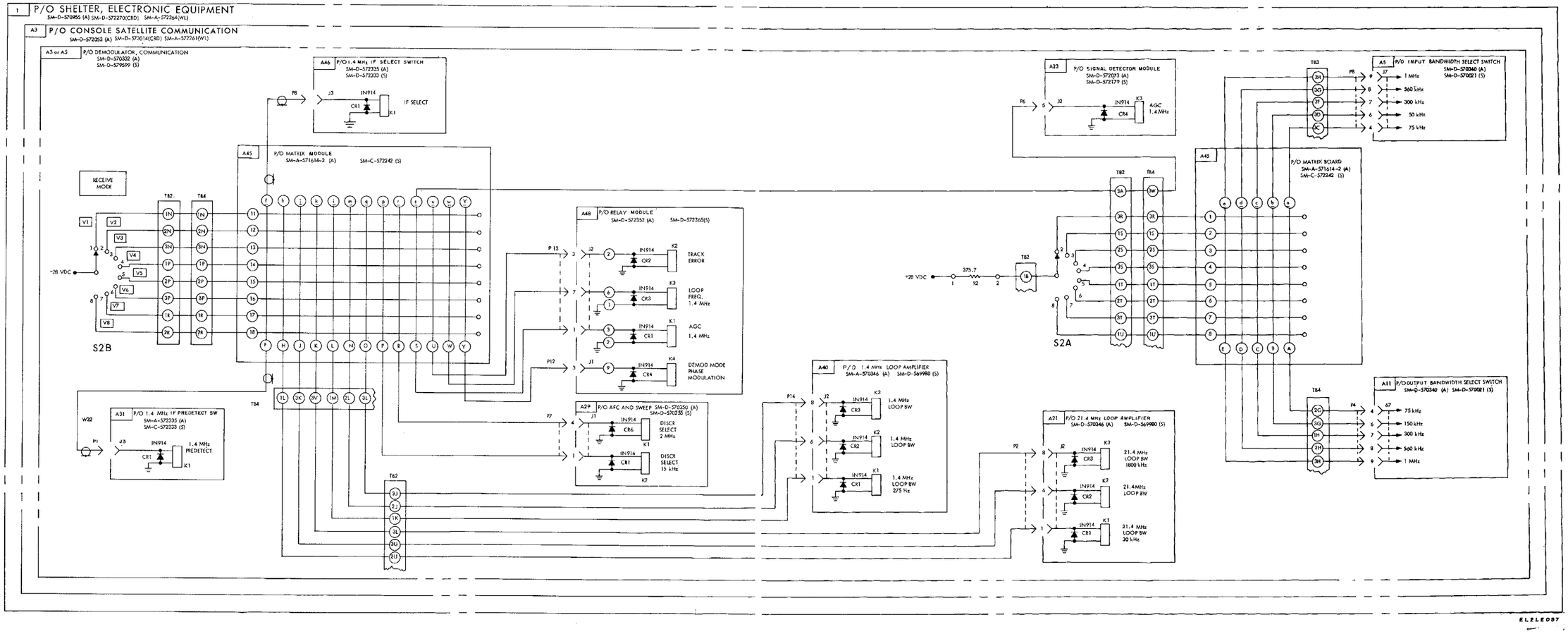

Figure FO 2-5 (5). Satellite Communication Terminal AN/TSC-54, receiving control and switching diagram (sheet 5 of 6).

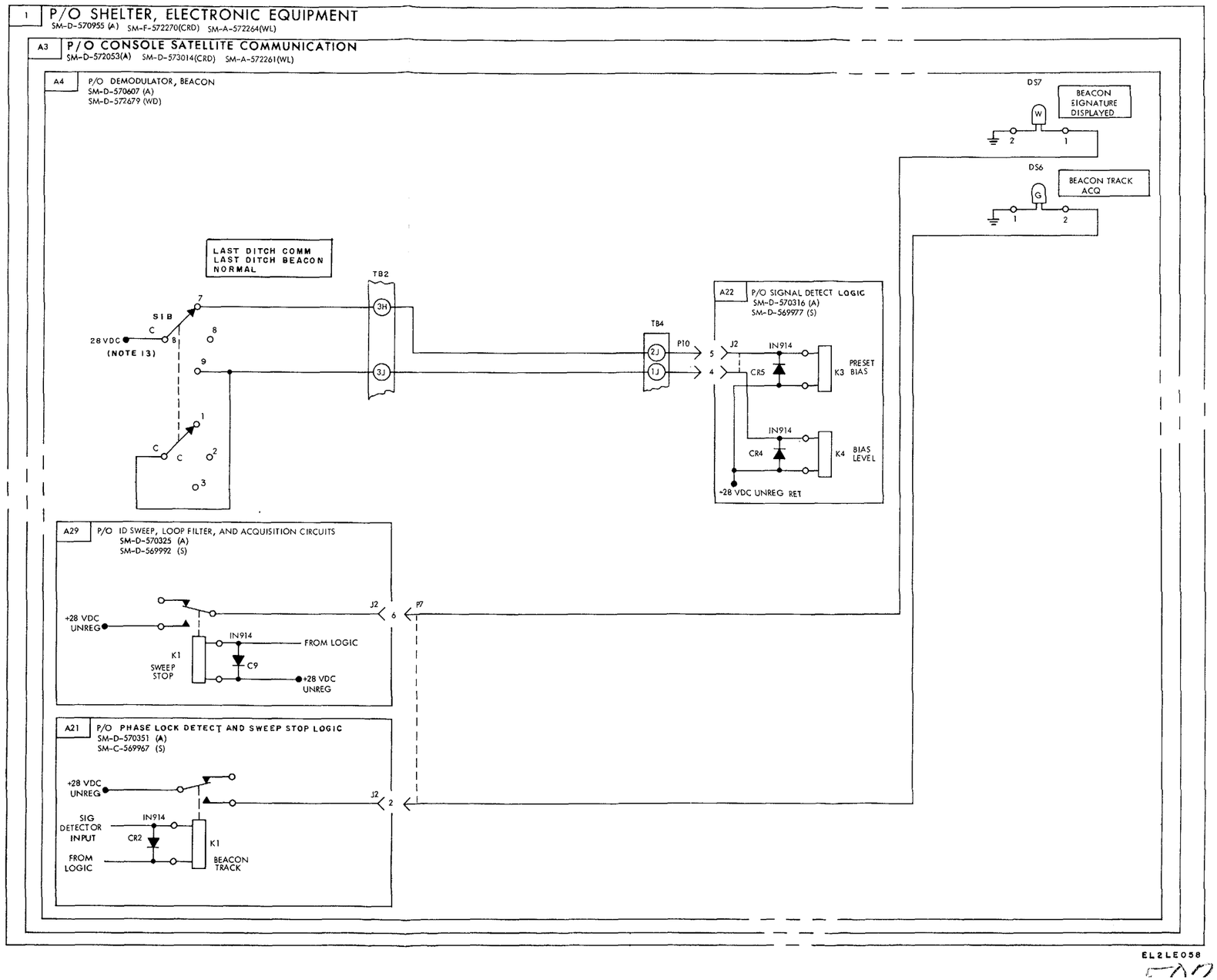

Figure FO 2-5(6). Satellite Communication Terminal AN/TSC-54, receiving control and switching diagram (sheet 6 of 6)

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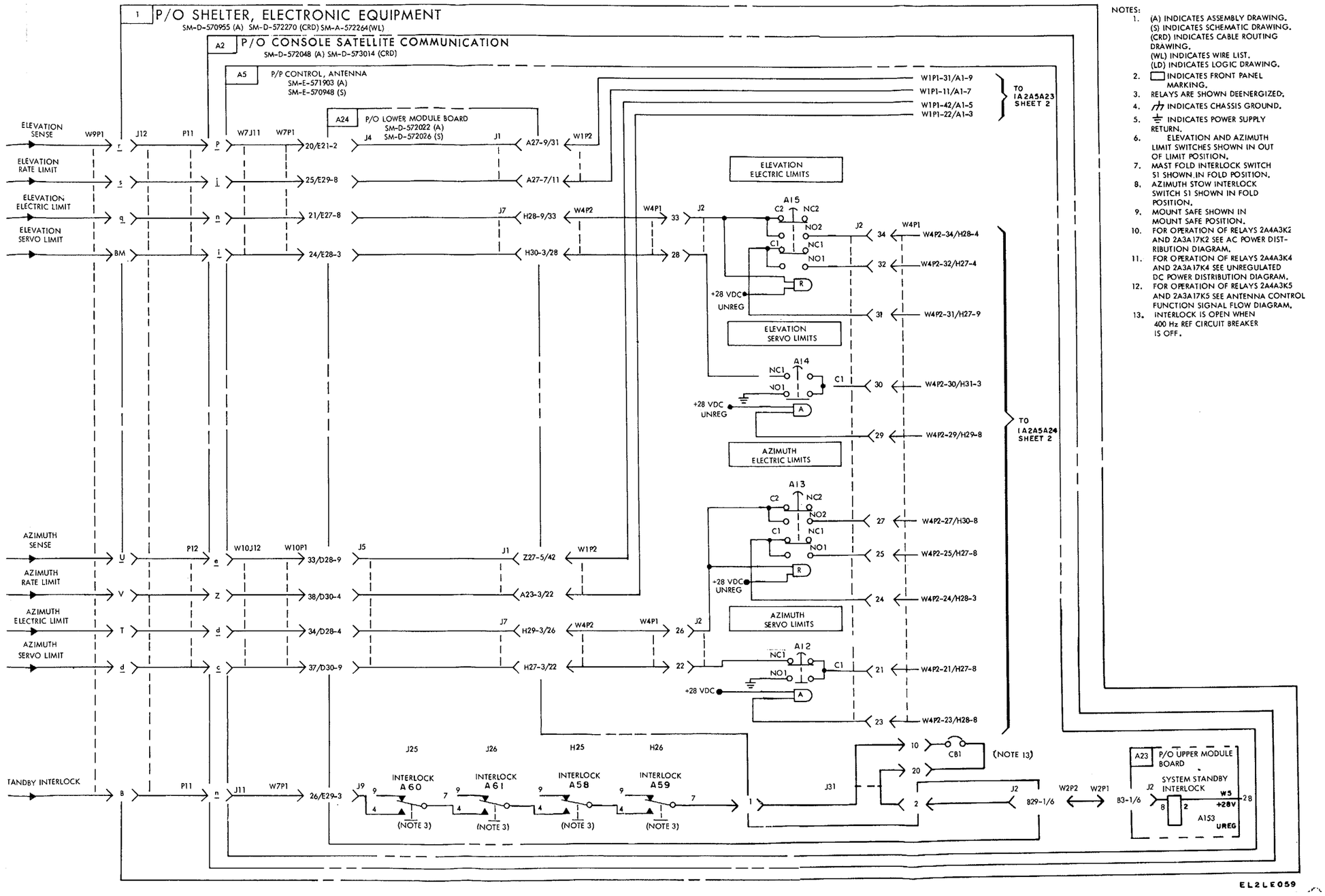

NOTES:
1. (A) INDICATES ASSEMBLY DRAWING. (S) INDICATES SCHEMATIC DRAWING. (CRD) INDICATES CABLE ROUTING DRAWING. (WL) INDICATES WIRE LIST. (LD) INDICATES LOGIC DRAWING.
2. ☐ INDICATES FRONT PANEL MARKING.
3. RELAYS ARE SHOWN DEENERGIZED.
4. ⏚ INDICATES CHASSIS GROUND.
5. ⏚ INDICATES POWER SUPPLY RETURN.
6. ELEVATION AND AZIMUTH LIMIT SWITCHES SHOWN IN OUT OF LIMIT POSITION.
7. MAST FOLD INTERLOCK SWITCH S1 SHOWN IN FOLD POSITION.
8. AZIMUTH STOW INTERLOCK SWITCH S1 SHOWN IN FOLD POSITION.
9. MOUNT SAFE SHOWN IN MOUNT SAFE POSITION.
10. FOR OPERATION OF RELAYS 2A4A3K2 AND 2A3A17K2 SEE AC POWER DISTRIBUTION DIAGRAM.
11. FOR OPERATION OF RELAYS 2A4A3K4 AND 2A3A17K4 SEE UNREGULATED DC POWER DISTRIBUTION DIAGRAM.
12. FOR OPERATION OF RELAYS 2A4A3K5 AND 2A3A17K5 SEE ANTENNA CONTROL FUNCTION SIGNAL FLOW DIAGRAM.
13. INTERLOCK IS OPEN WHEN 400 Hz REF CIRCUIT BREAKER IS OFF.

Figure FO 2-6 (1). Satellite Communication Terminal AN/TSC-54, antenna control and switching diagram (sheet 1 0f 6)

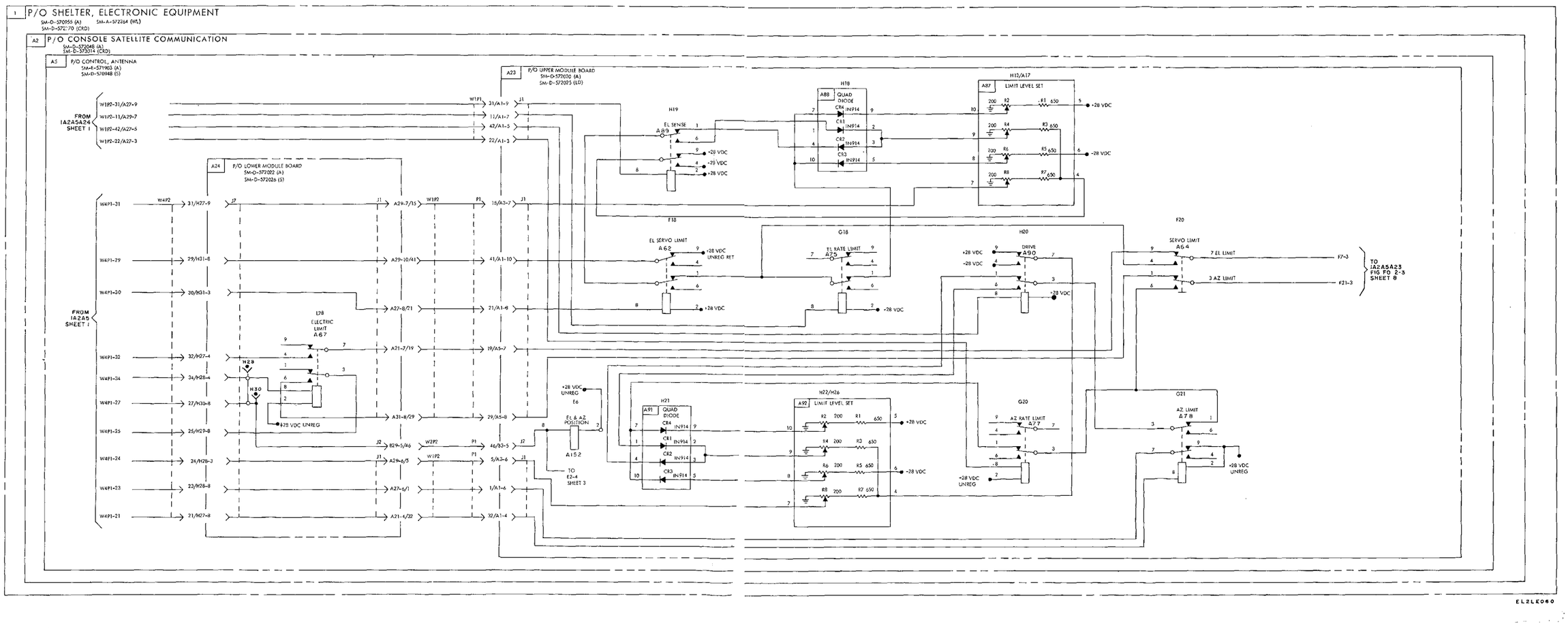

Figure FO 2-6 (2). Satellite Communication Terminal AN/TSC-54, antenna control and switching, signal flow diagram (Sheet 2 of 6)

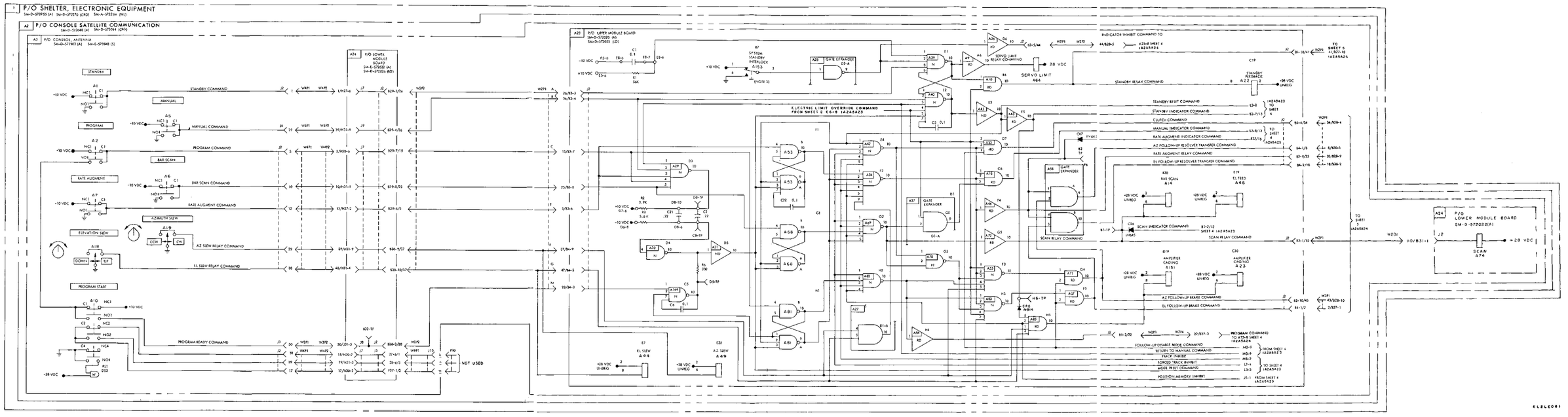

Figure FO 2-6 (3). Satellite Communication Terminal AN/TSC-54, antenna control and switching, signal flow diagram (Sheet 3 of 6)

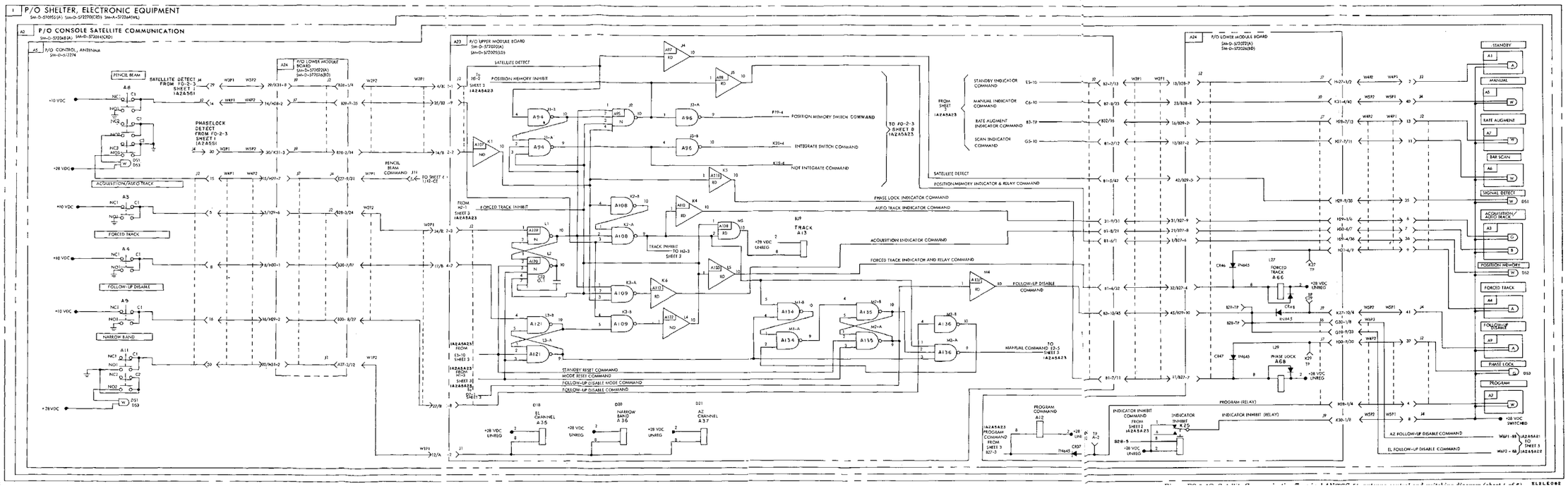

Figure FO 2-6 (4). Satellite Communication Terminal AN/TSC-54, antenna control and switching, signal flow diagram (Sheet 4 of 6)

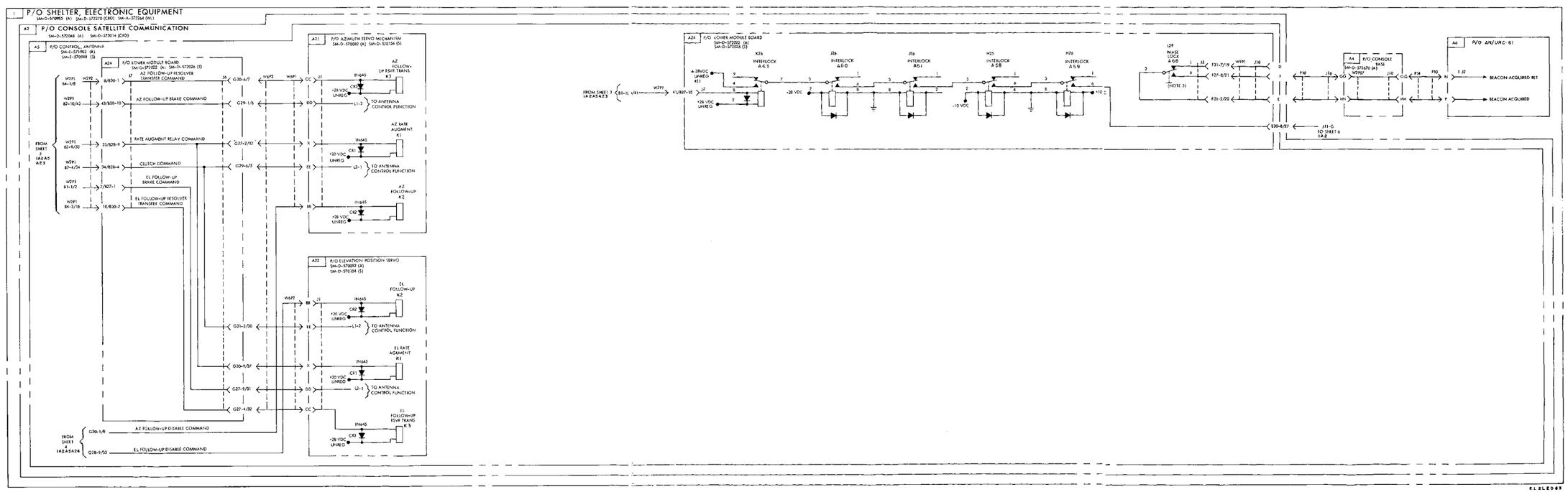

Figure FO 2-6 (5). Satellite Communication Terminal AN/TSC-54, antenna control and switching, signal flow diagram (Sheet 5 of 6)

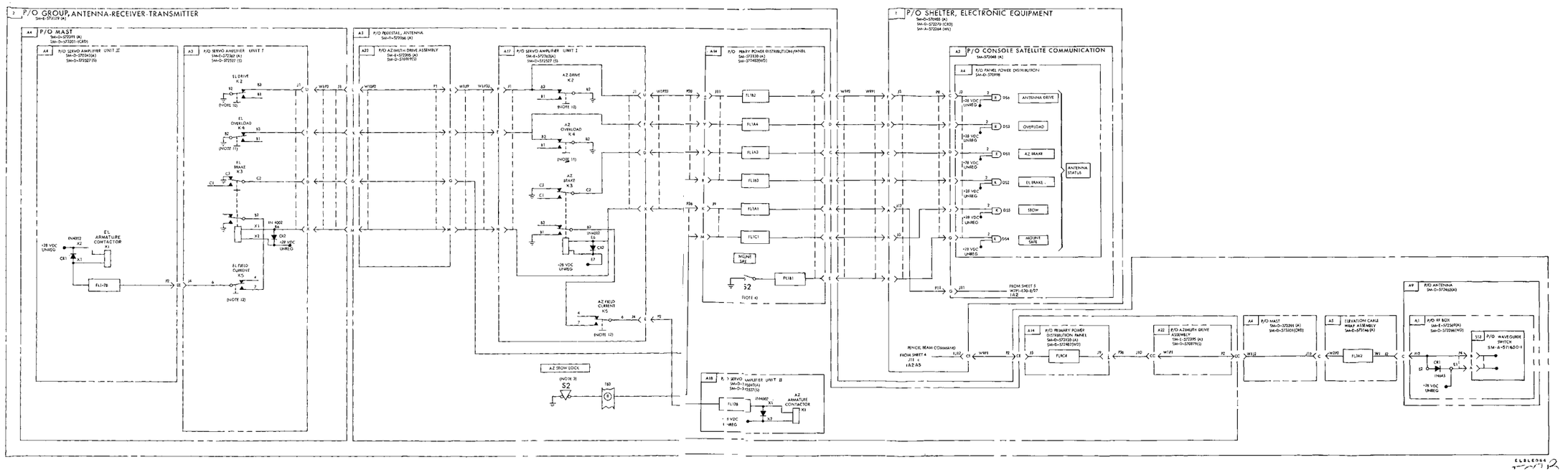

Figure FO 2-6 (6). Satellite Communication Terminal AN/TSC-54, antenna control and switching, signal flow diagram (Sheet 6 of 6)

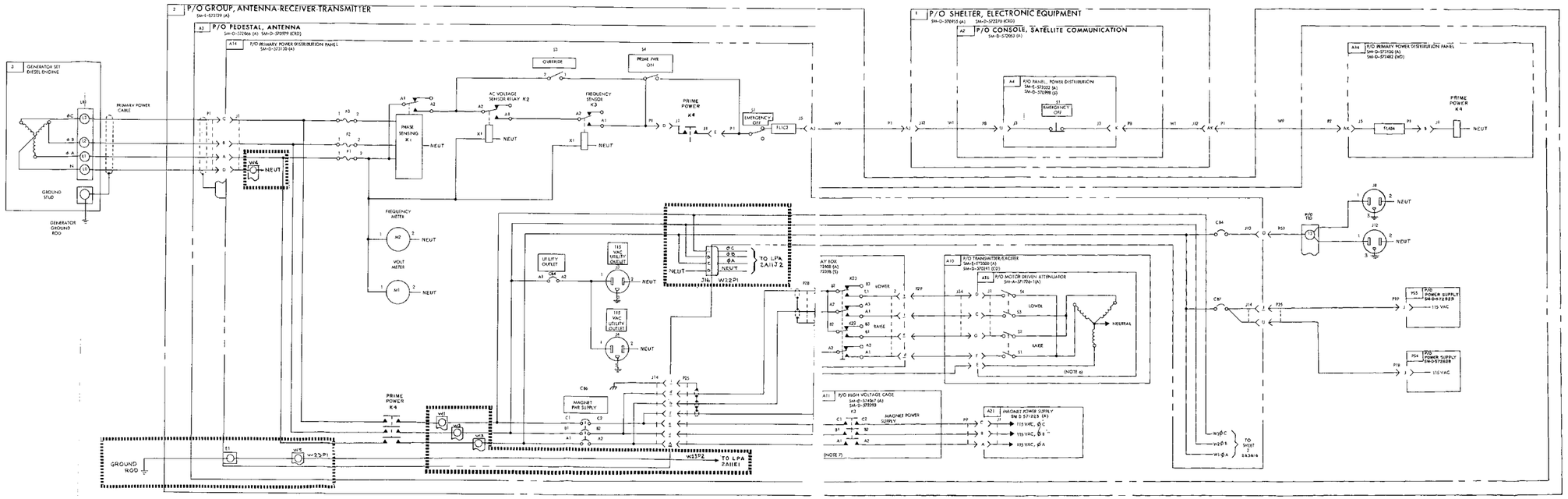

Figure FO-2-7. Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 1 of 9)

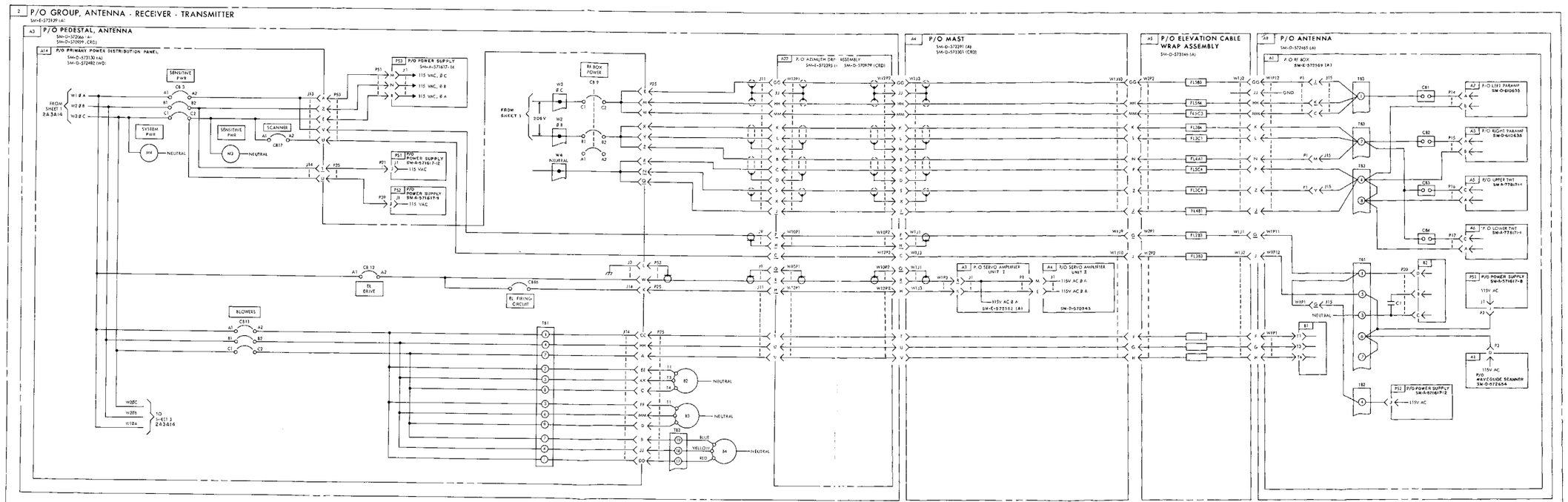

Figure FO-2-7. Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 2 of 9)

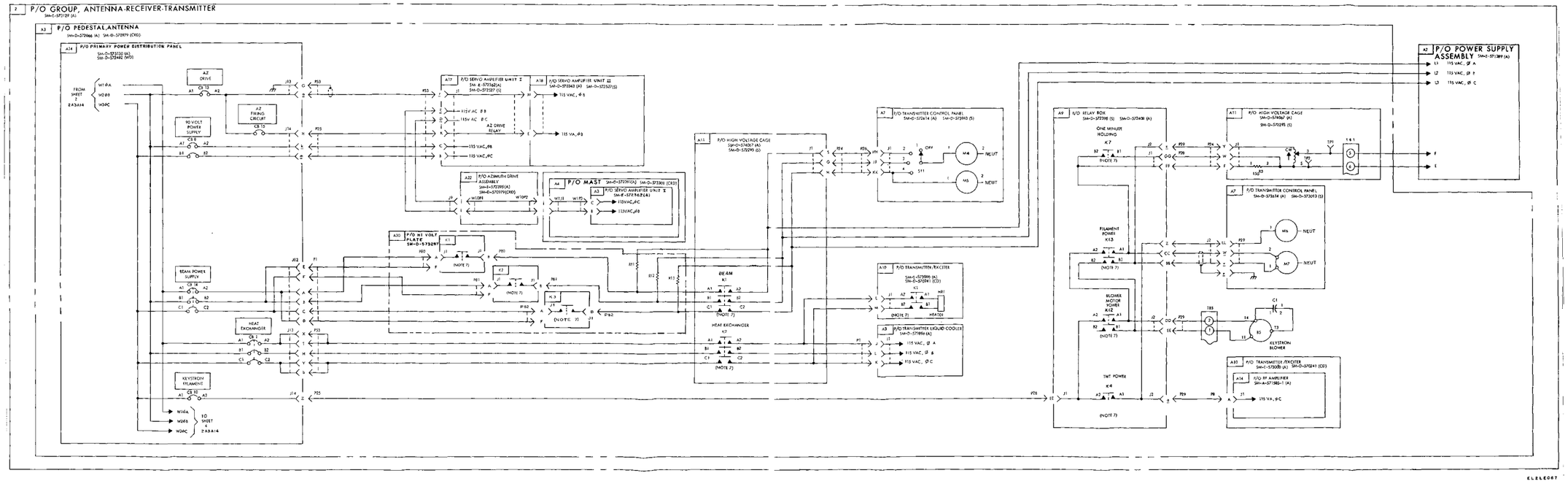

Figure FO-2-7. Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 3 of 9)

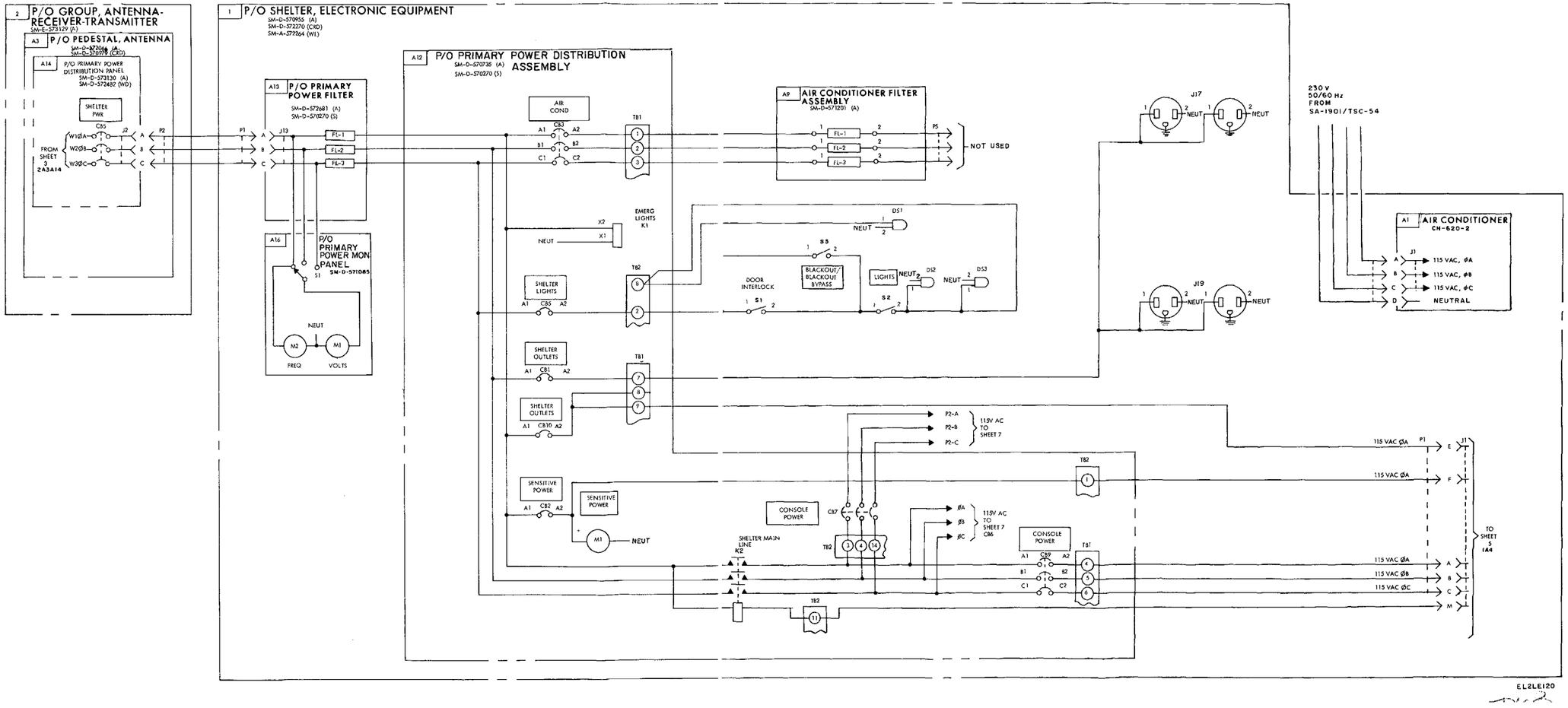

Figure FO-2-7. Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 4 of 9)

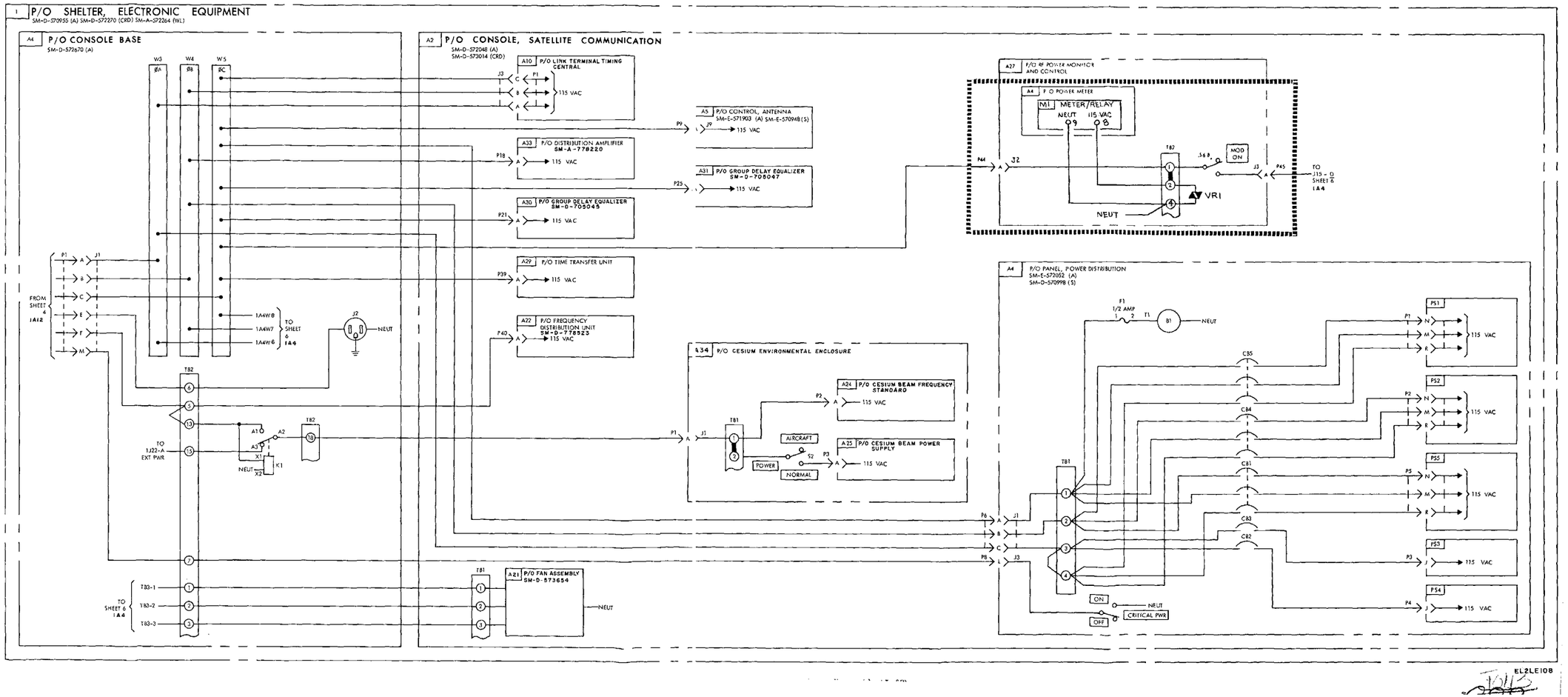

Figure FO-2-7. Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 5 of 9)

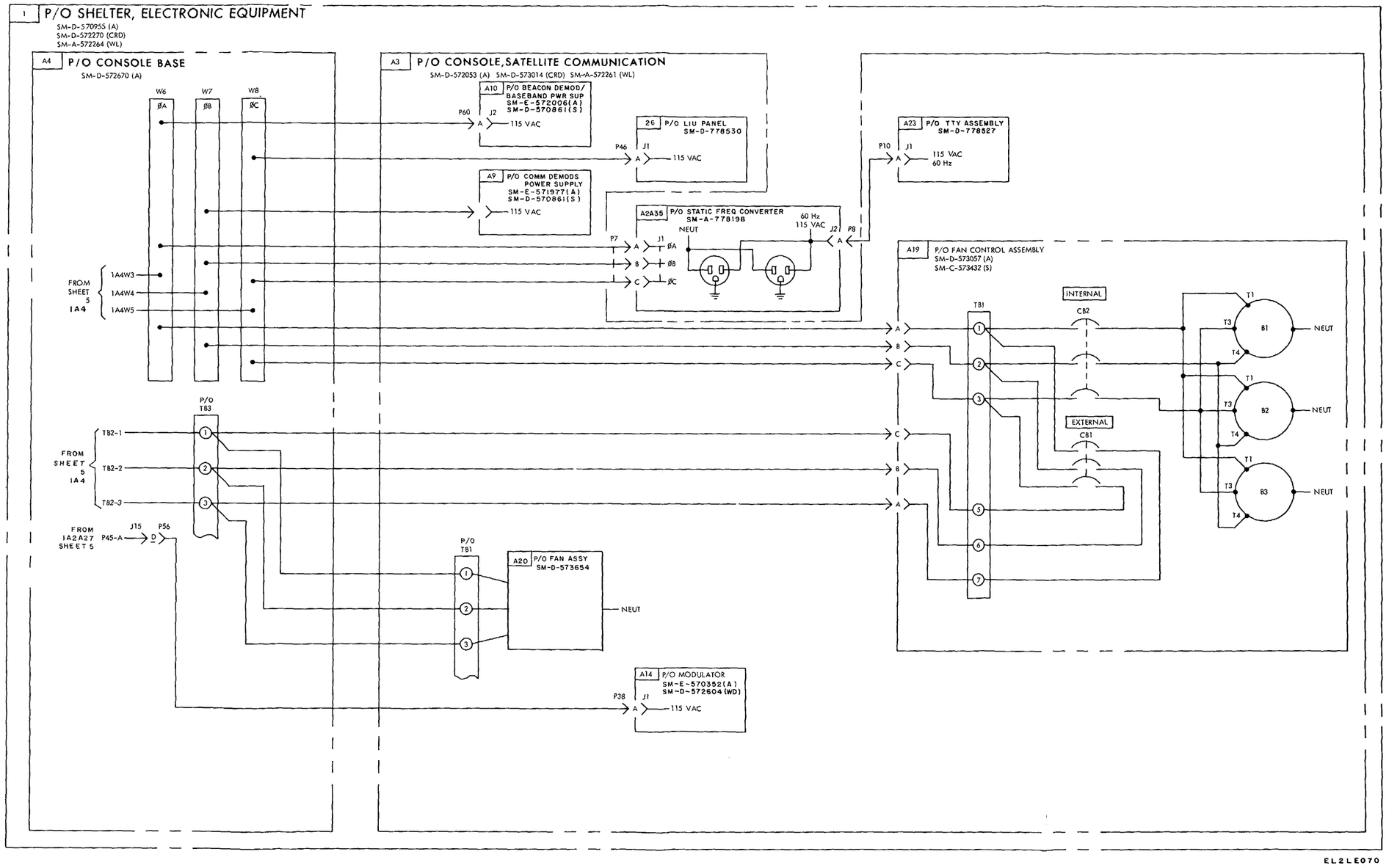

Figure FO 2-7(6). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 6 of 9).

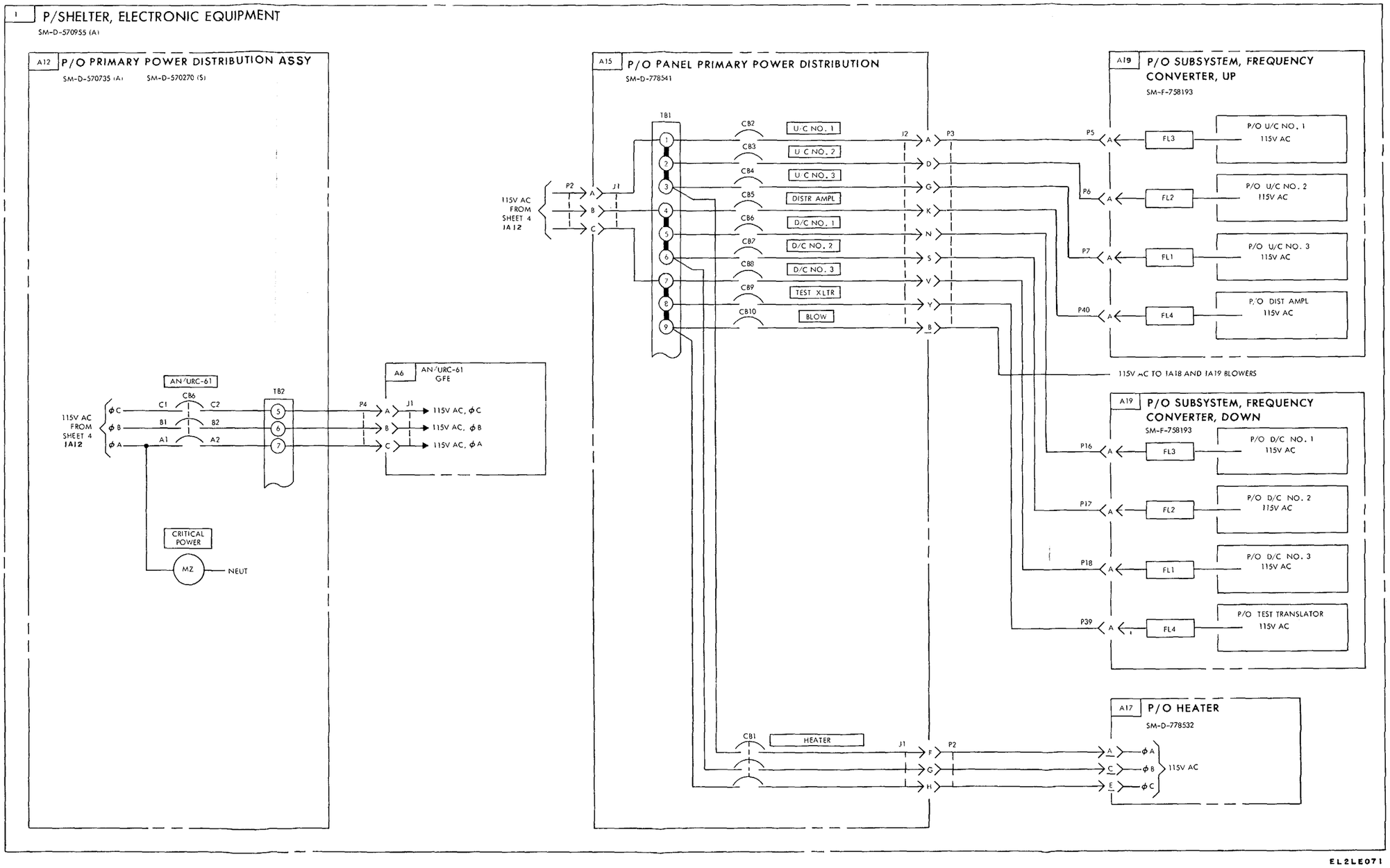

Figure FO 2-7(7). Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 7 of 9).

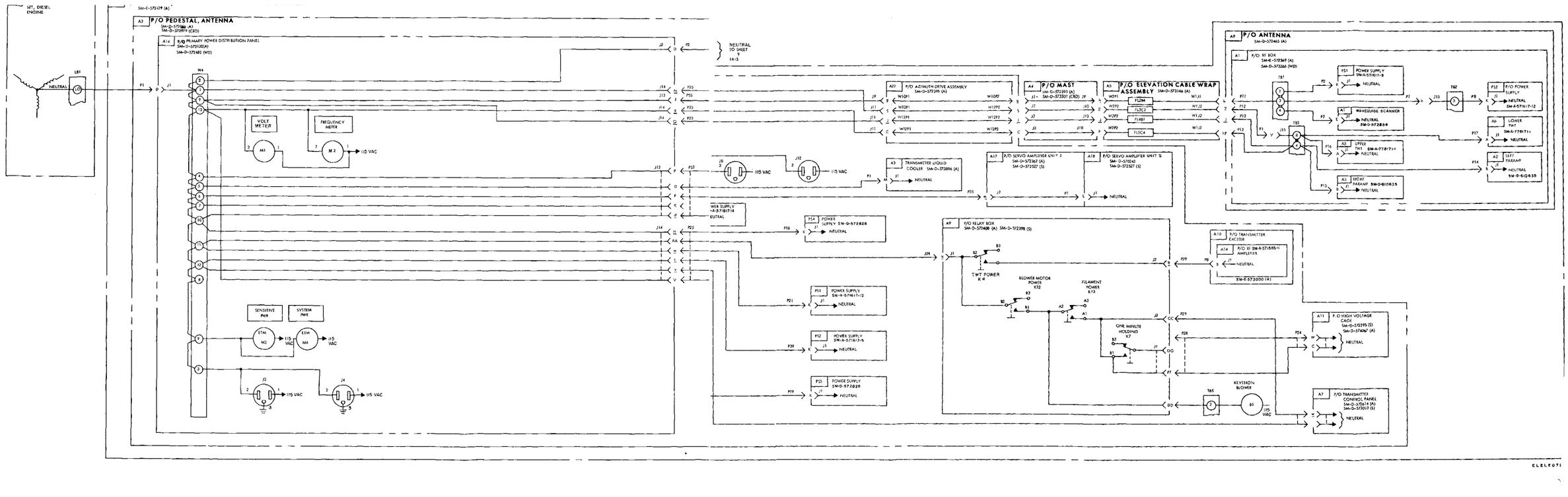

Figure FO 2-7(8). Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 8 of 9).

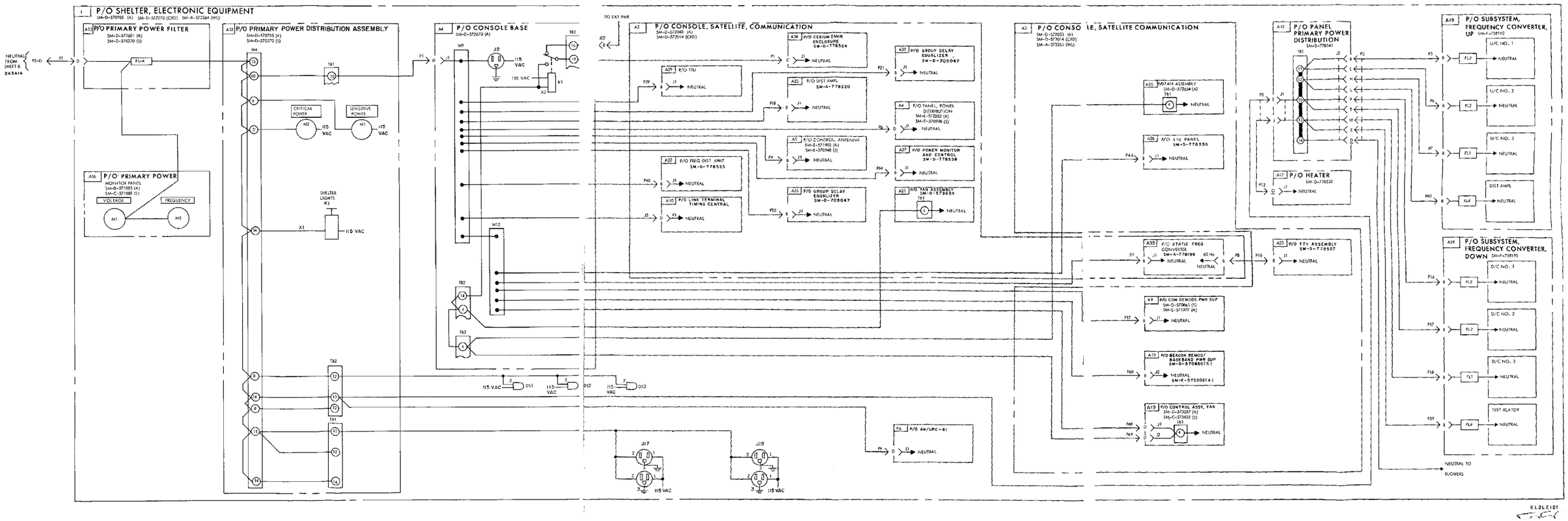

Figure FO 2-7. Satellite Communication Terminal AN/TSC-54, ac power distribution diagram (sheet 9 of 9).

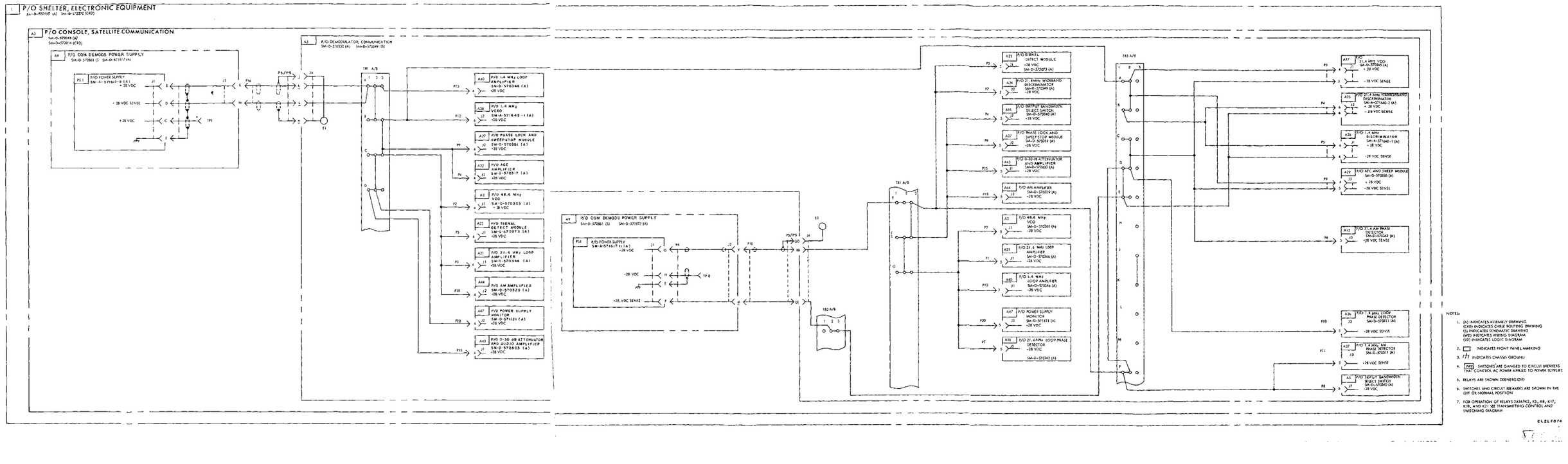

Figure FO 2-8(1). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 1 of 10).

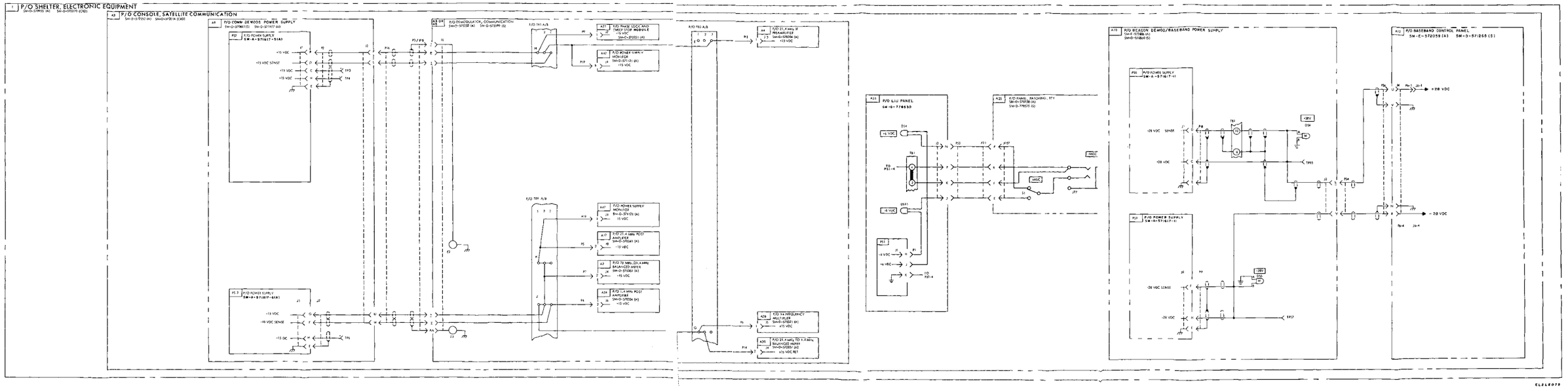

Figure FO 2-8(2). Satellite Commercial Terminal AN/TSC-54, dc power distribution diagram (sheet 2 of 10)

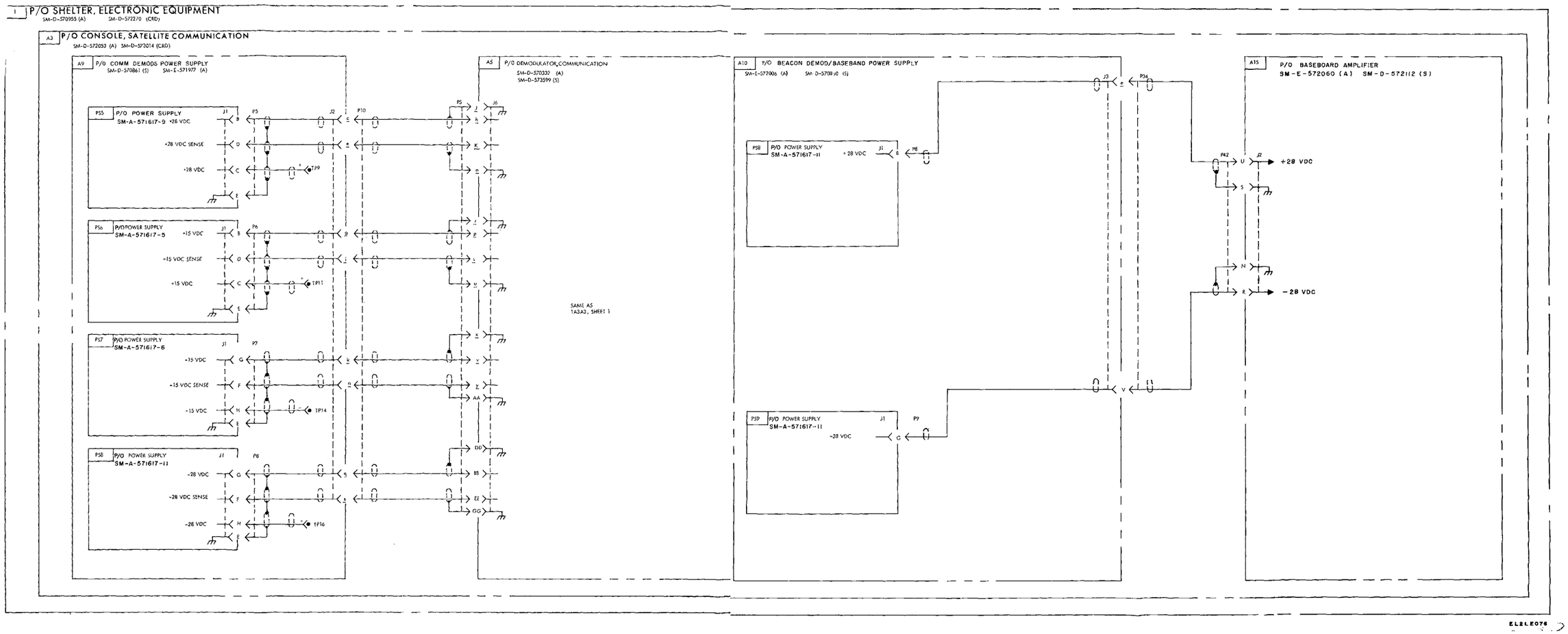

Figure FO 2-8(3). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 3 of 10)

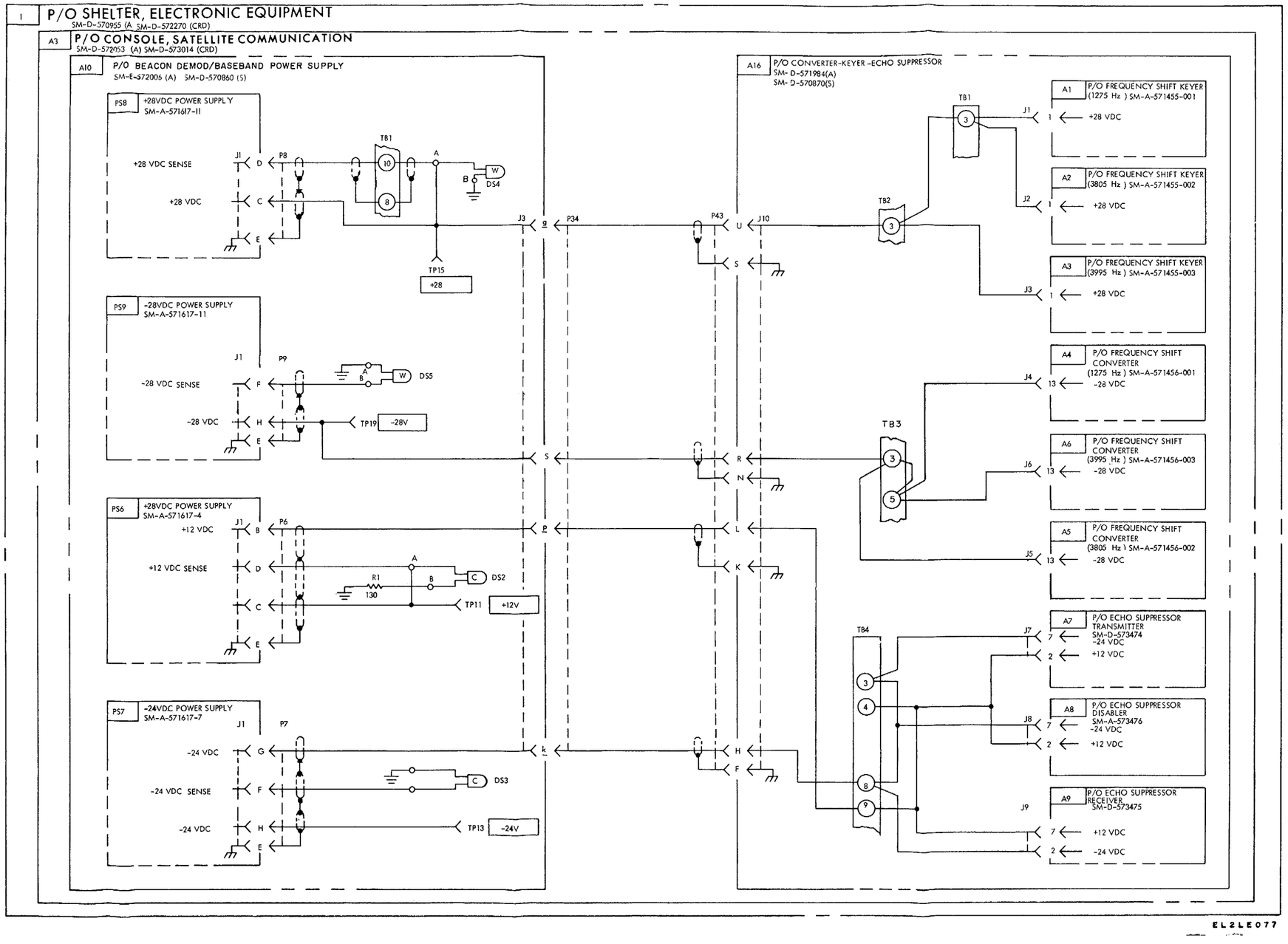

Figure FO 2-8(4). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 4 of 10)

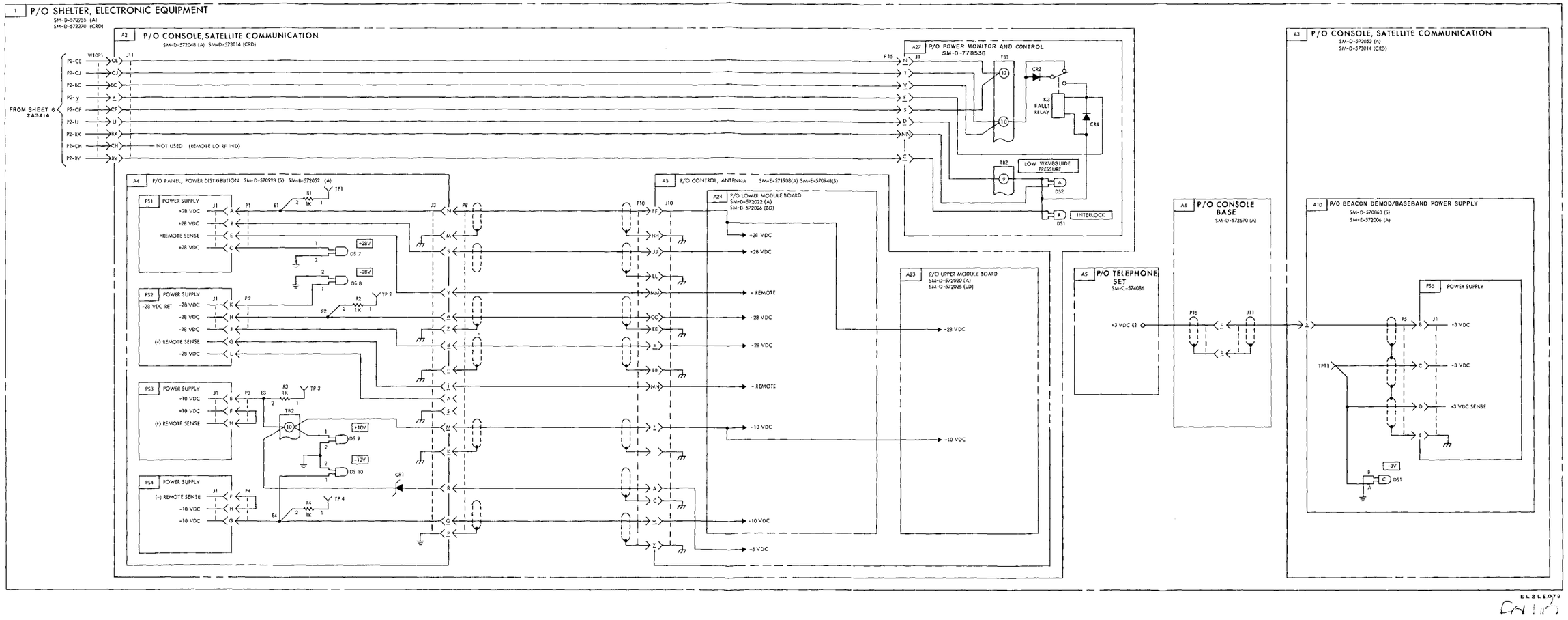

Figure FO 2-8(5). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 5 of 10).

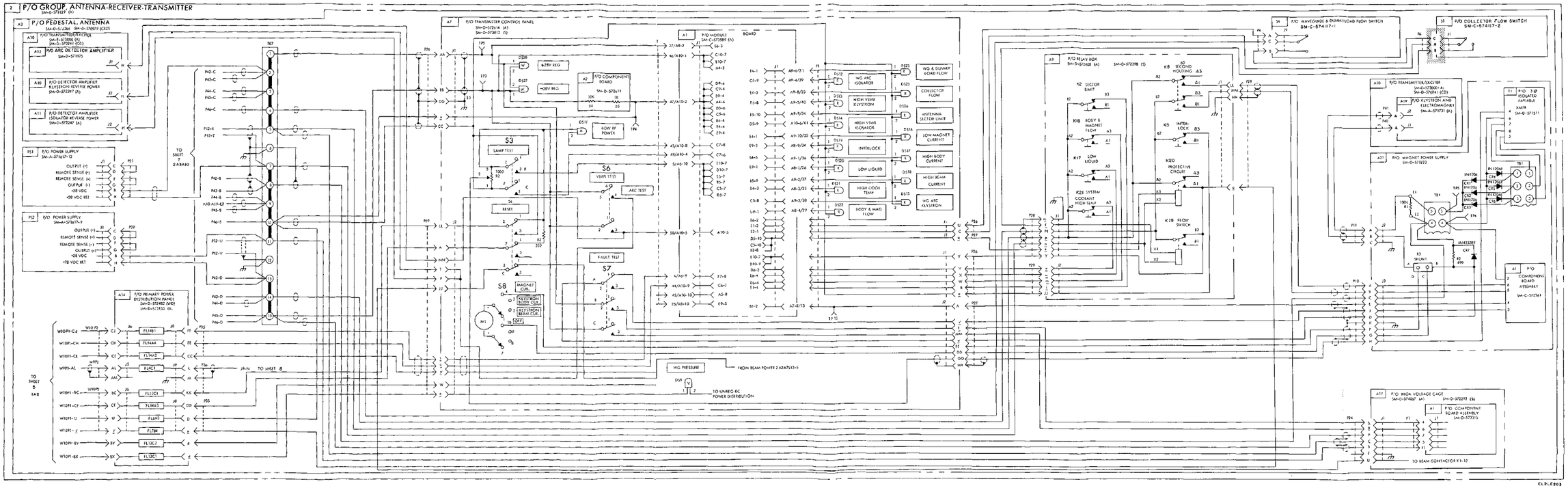

Figure 2-8. Satellite Communication Terminal AN/TSC-54, regulated dc power distribution diagram (sheet 6 of 10).

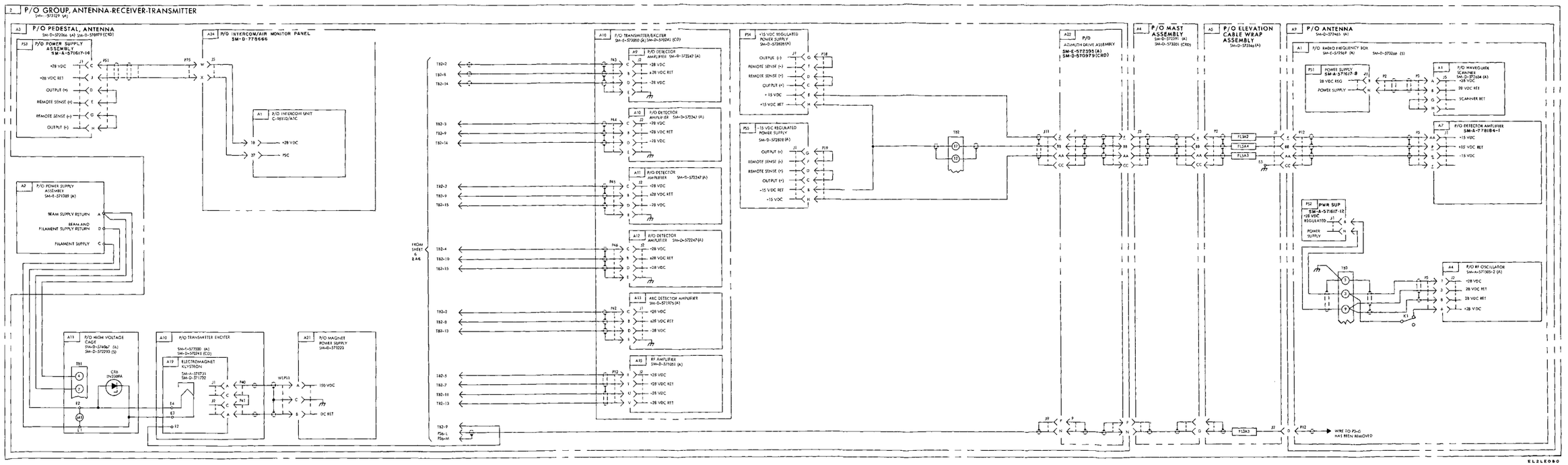

Figure FO 2-8 (7). Satellite Communication Terminal AN/TSC-54, dc power distribution (sheet 7 of 10).

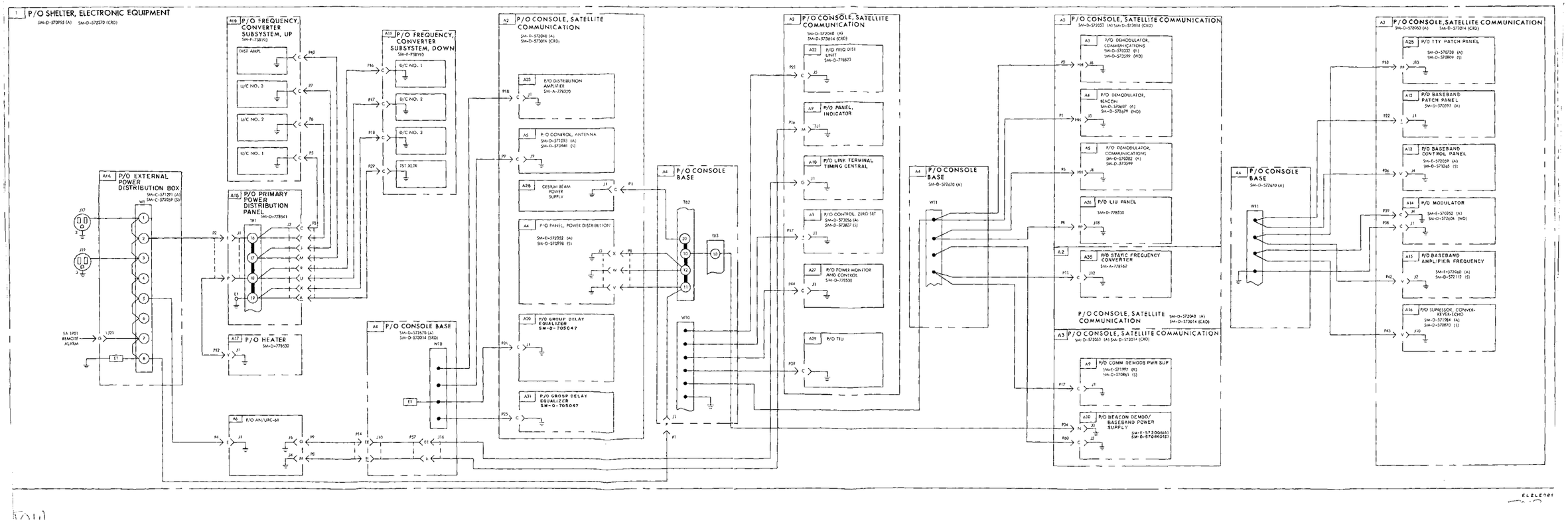

Figure FO 2-8(8). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 8 of 10).

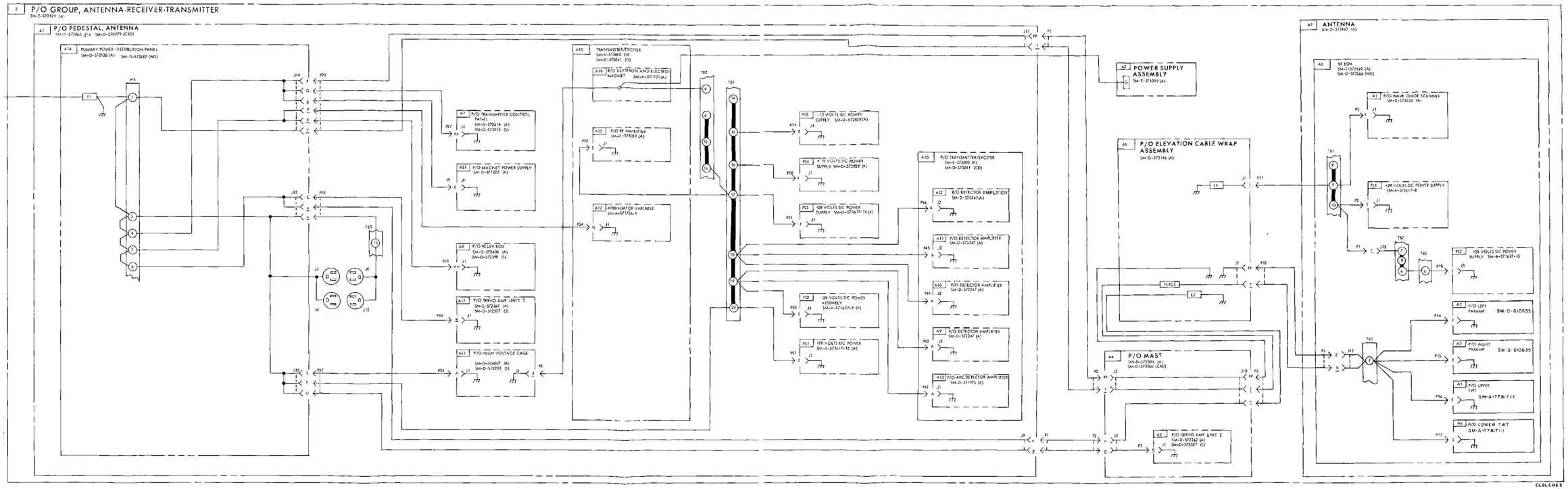

Figure FO 2-8. (9). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 9 of 10).

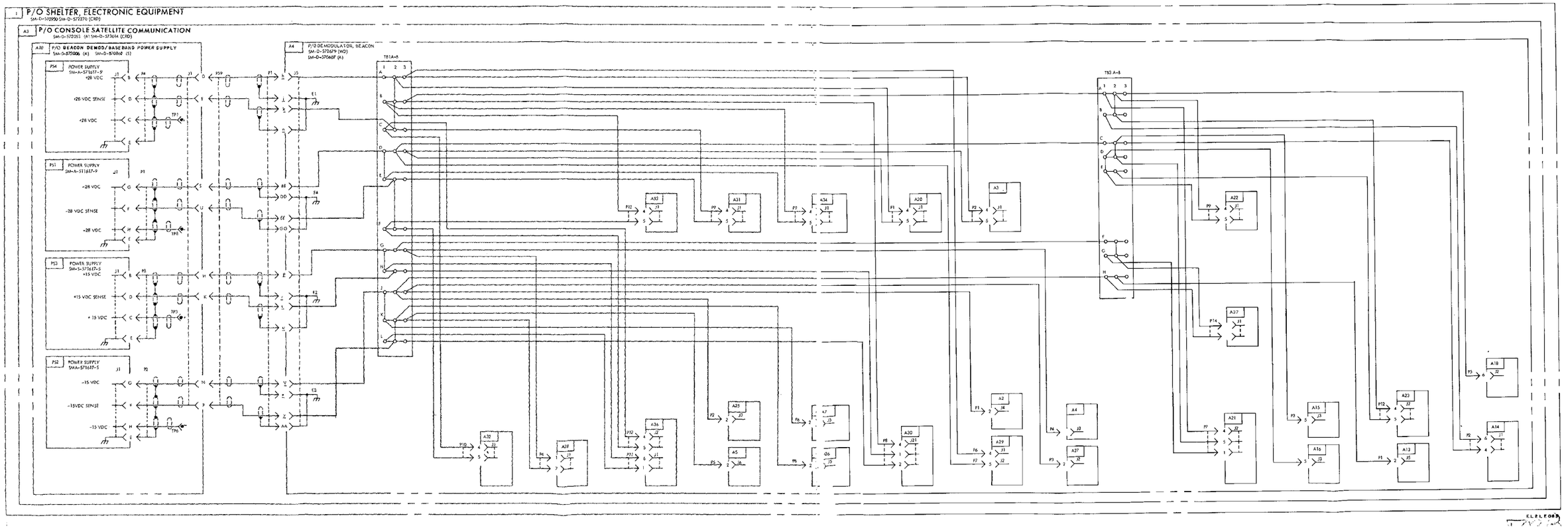

Figure FO 2-8. (10). Satellite Communication Terminal AN/TSC-54, dc power distribution diagram (sheet 10 of 10).

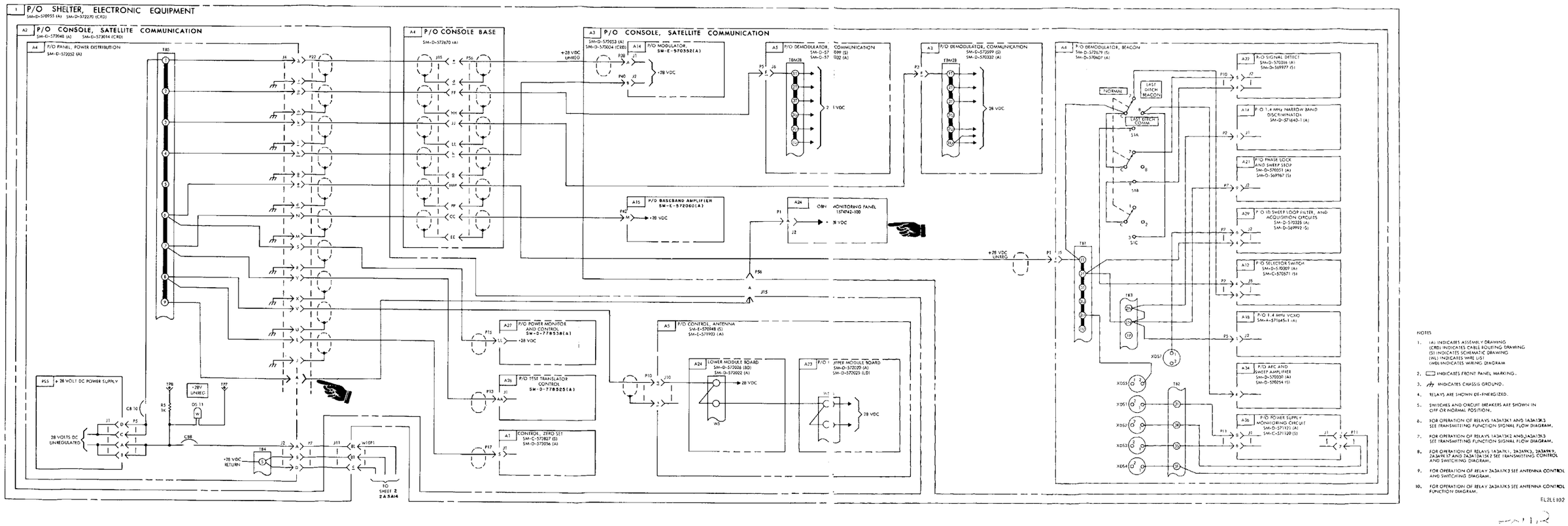

Figure FO 2-9 (1). Satellite Communication Terminal AN/TSC-54, unregulated dc power distribution diagram. (sheet 1 of 3)

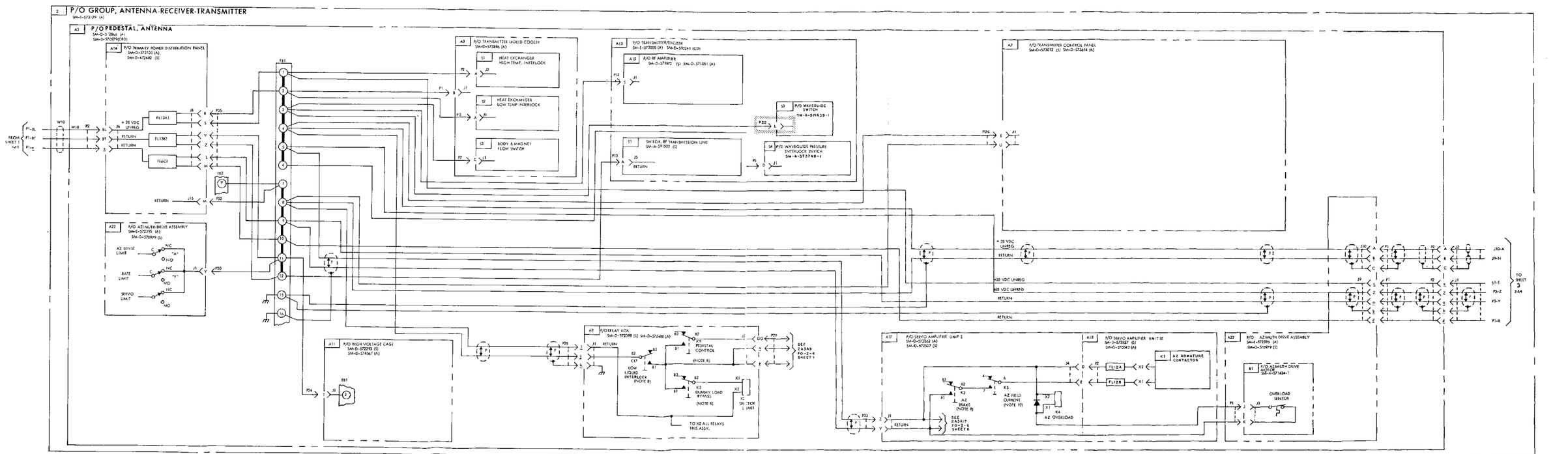

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Figure FO-2-9. Satellite Communication Terminal AN/TSC-54, unregulated dc power distribution diagram (sheet 2 of 3).

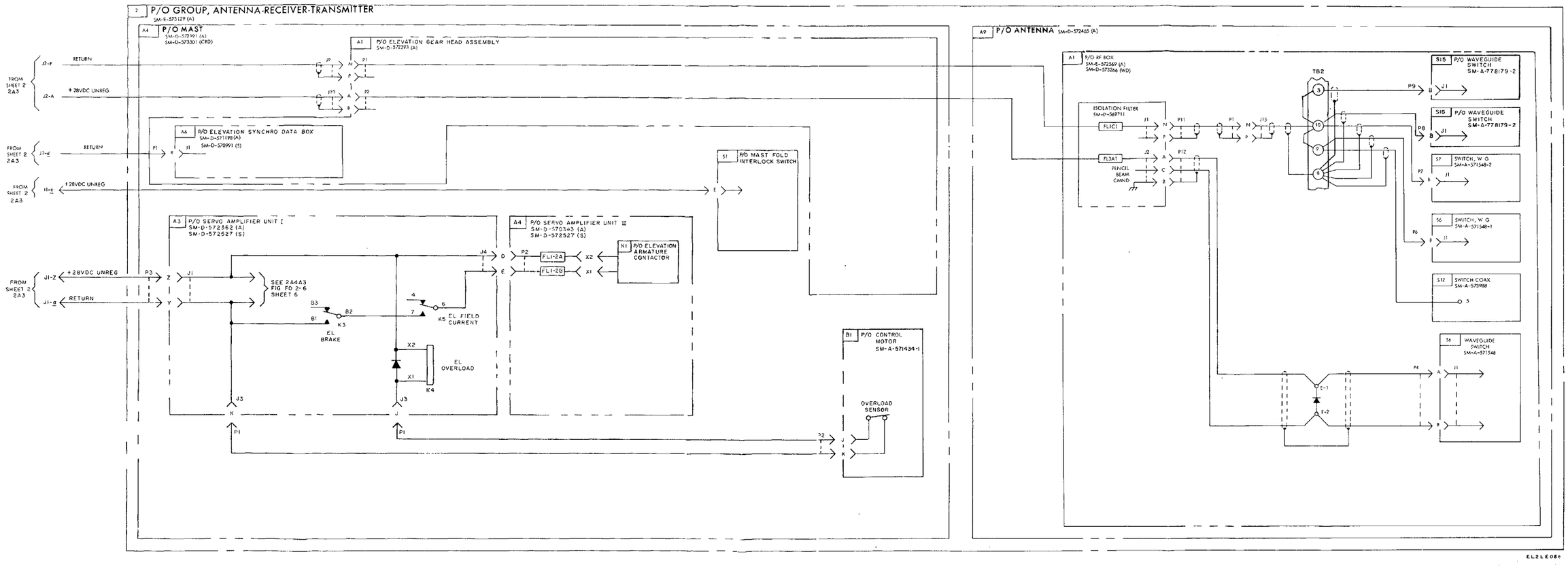

Figure FO 2-9. Satellite Communication Terminal AN/TSC-54, unregulated dc power distribution diagram (sheet 3 of 3).

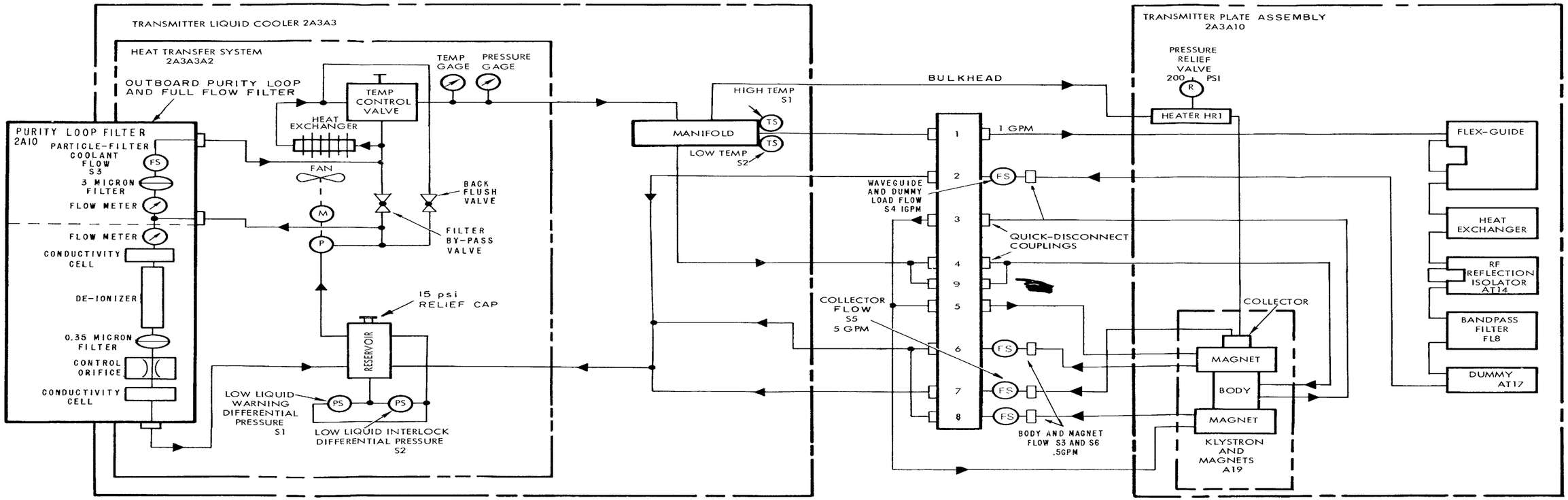

Figure FO 2-10. Transmitter cooling system, flow diagram.

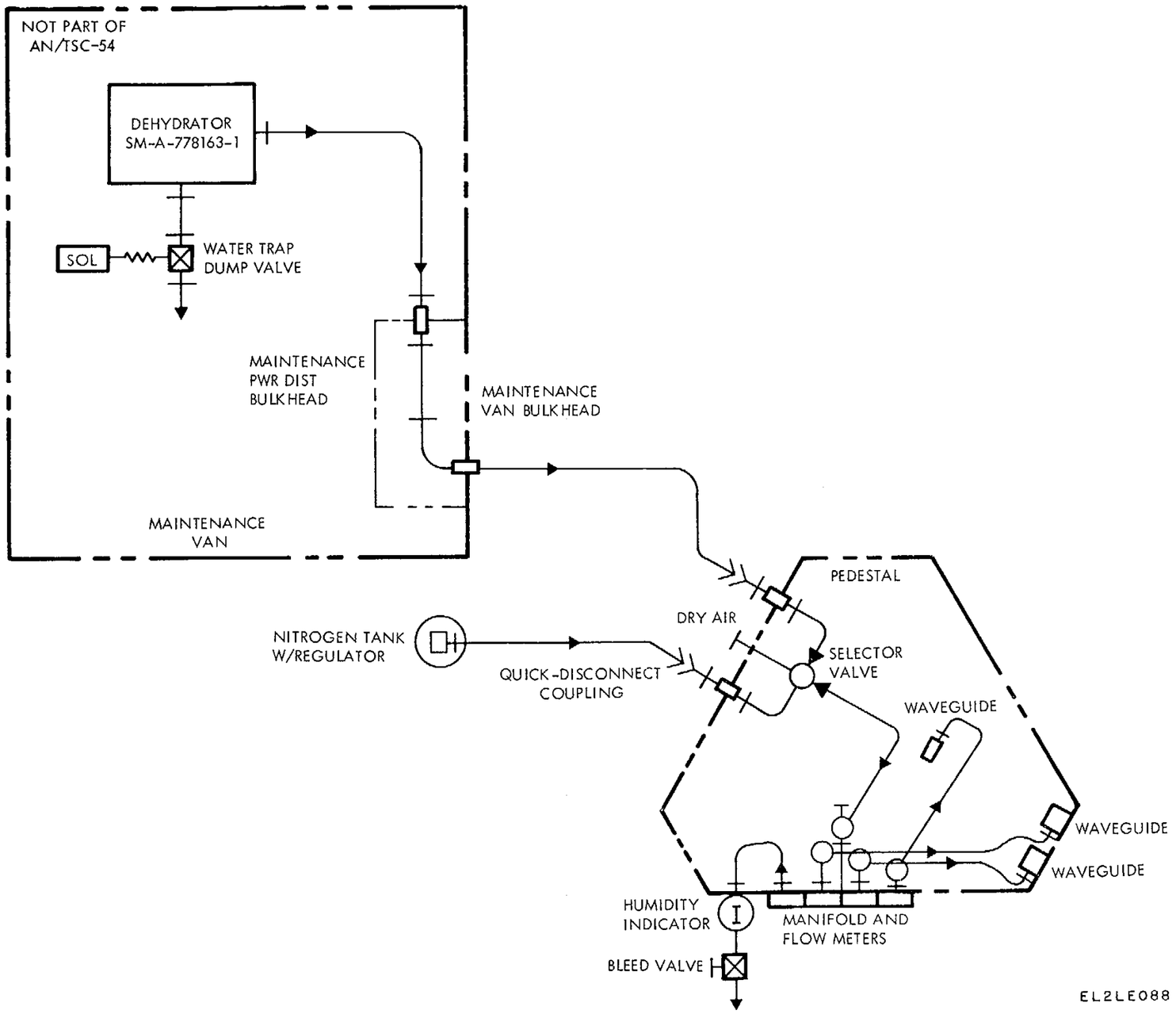

Figure FO 2-11. Waveguide pressurization system, flow diagram.

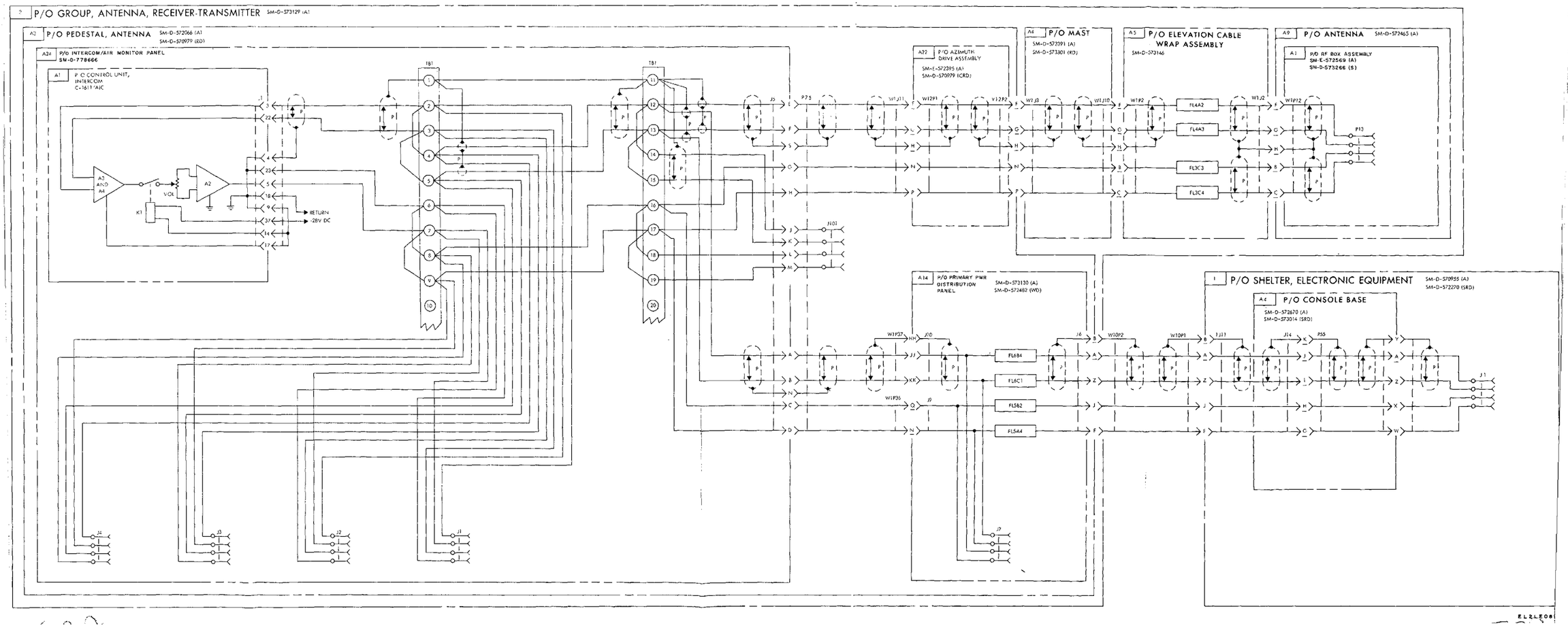

Figure FO 2-12. Satellite Communication Terminal AN/TSC-54, intercom system diagram.

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